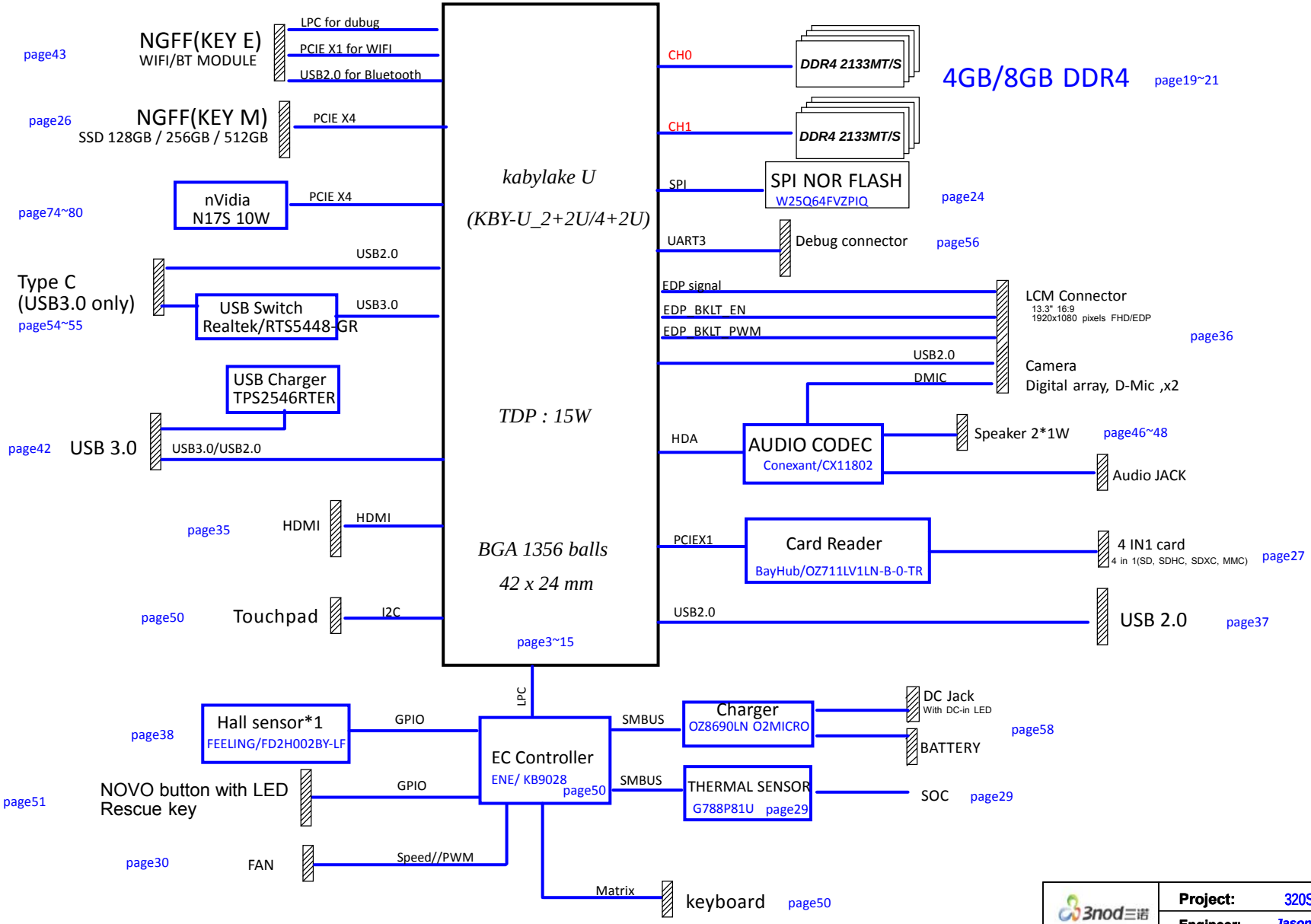
320S-13 for Lenovo



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: COVER PAGE	Rev: V01
Date: Monday, April 10, 2017	Sheet 1 of 81	

TABLE OF CONTENTS

01 -- COVER PAGE
02 -- TABLE OF CONTENTS
03--SKL-U(1/12)DDI,MISC,XDP,EDP
04--SKL-U(2/12)DDR4
05--SKL-U(3/12)SPI,ESPI,SMB,LPC
06--SKL-U(4/12)HDA,EMMC,SD
07--SKL-U(5/12)CLK,GPIO
08--SKL-U(6/12)GPIO
09--SKL-U(7/12)PCIE,USB,SATA
10--SKL-U(8/12)Power
11--SKL-U(9/12)Power
12--SKL-U(10/12)Power,SVID
13--SKL-U(11/12)GND
14--SKL-U(12/12)RSVD
15--SOC (DECOUPLING)
16--NA
17--NA
18--NA
19--DDR4_CHA
20--DDR4_CHB
21--DDR4 Decoupling
22--NA
23--RF / EMC Solution
24 -- SYSTEM FLASH
25 -- NC_EMMC
26 -- PCIE SSD MODULE
27 -- NC_MICRO-SD CARD
28 -- NC_SD CARD POWER
29 -- CPU THERMAL SENSOR
30 -- FAN conn
31 -- NA
32 -- NA
33 -- NA
34 -- NC_HDMI LEVEL SHIFTERS
35 -- NC_HDMI CONNECTOR
36 -- DISPLAY
37 -- TOUCH PANEL AND DOCK
38 -- SENSORS & LID
39 -- FRONT AND REAR CAMERA CON
40 -- CAMERA DISCRETE CONTROLL
41 -- TPM
42 -- USB3.0 CONN
43 -- WLAN WIFI BT MODULE
44 -- WWAN MODULE
45 -- MICRO SIM
46 -- AUDIO CODEC
47 -- AUDIO-MIC AND SPKRS
48 -- IO board CONN
49 -- DC JACK
50 -- EMBEDDED CONTROLLER
51 -- BUTTON & LED
52 -- TYPE-C MULTIPLEXER
53 -- TYPE-C PD CONTROLLER
54 -- NC_TYPE-C BOOST VR
55 -- TYPE-C CONNECTOR
56 -- UART CONN & HOLE & CLIP
57 -- HW Change list
58--PWR_DCIN/BATT CONN
59--PWR_CHARGER(OZ8690)
60--PWR-+V5P0A / +V3P3A
61--PWR-DDR
62--PWR-+V2P5U_VPP
63--PWR-+1.0V_PRIM
64--PWR-NA
65--PWR-+1.8V_PRIM
66--PWR-CPU VR IC
67--PWR-VCC_CORE/GT/SA
68--PWR-Block Diagram
69--PWR_Change list

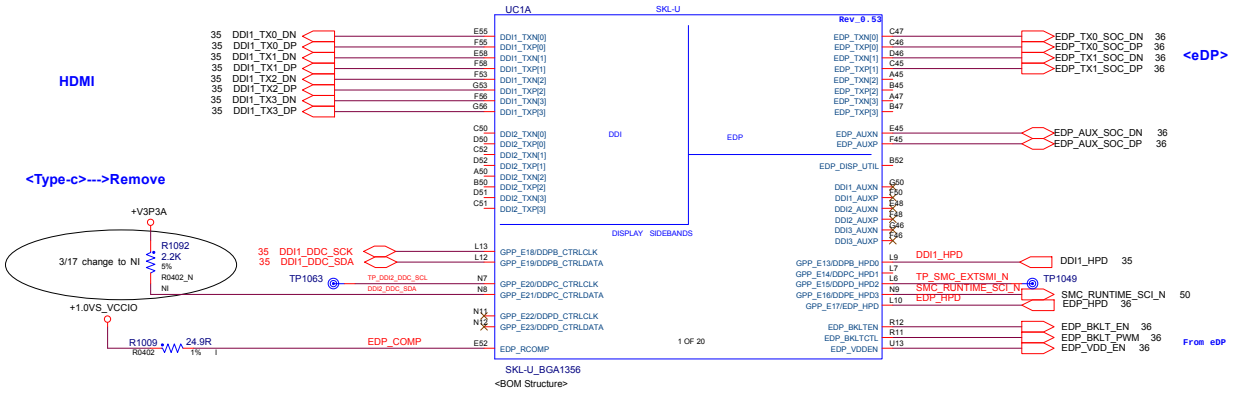
INTERNAL ONLY

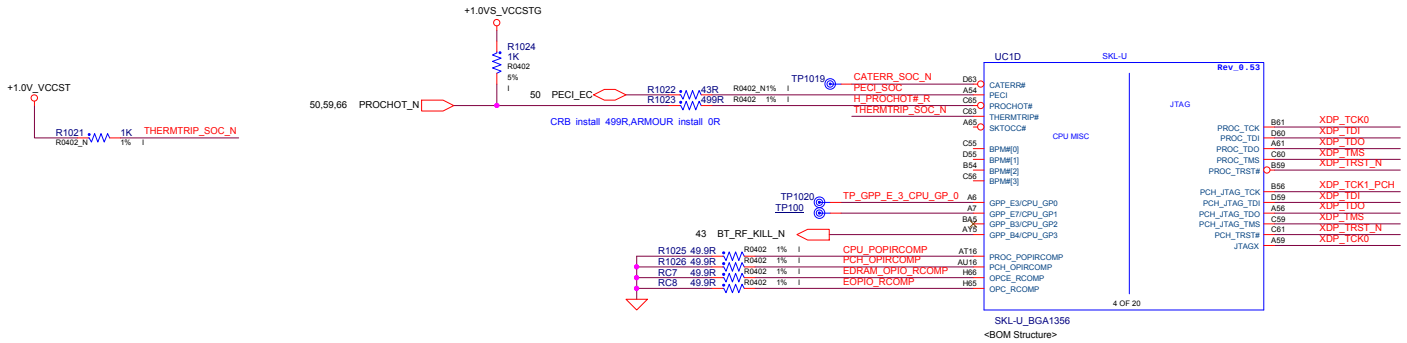
BPAGE DRAWING

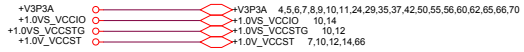
sky_y_mrd:_
Wed Jun 03 11:22:42 2015

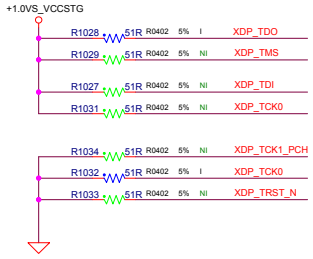
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
Date: Monday, April 10, 2017	Sheet 2 of 81	

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.



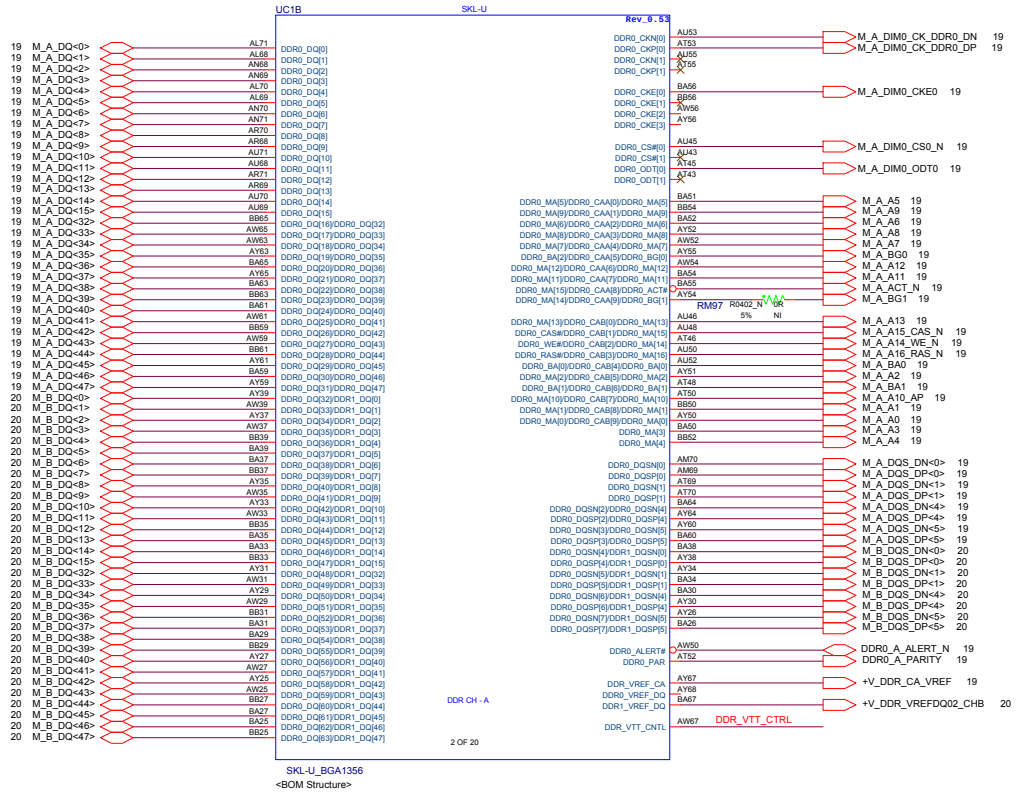




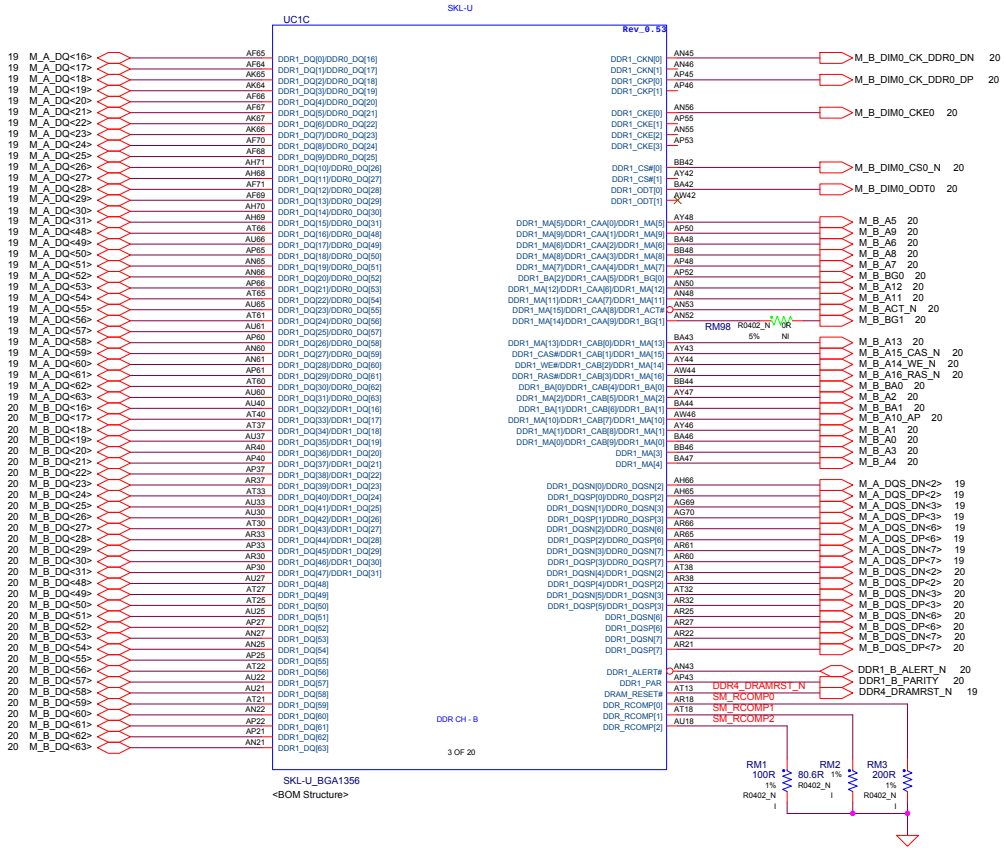


3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(1/12)DDI,MISC,XDP,EDP	Rev: V01
Date: Monday, April 10, 2017	Sheet 3 of 81	

Non-Interleaved



Non-Interleaved



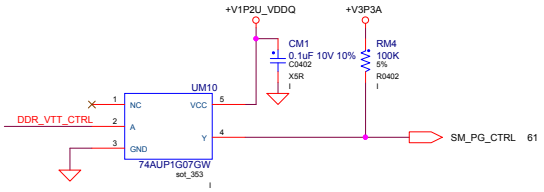
1. To support DDP, need to change two pins on DRAM. You have reserved them. Pls install the BOM.

	X16 SDP	X16 DDP TwinDie
DRAM M9 pin	VSS	Connect to CPU BG1
DRAM E9 Pin	VSS	UZQ

Default

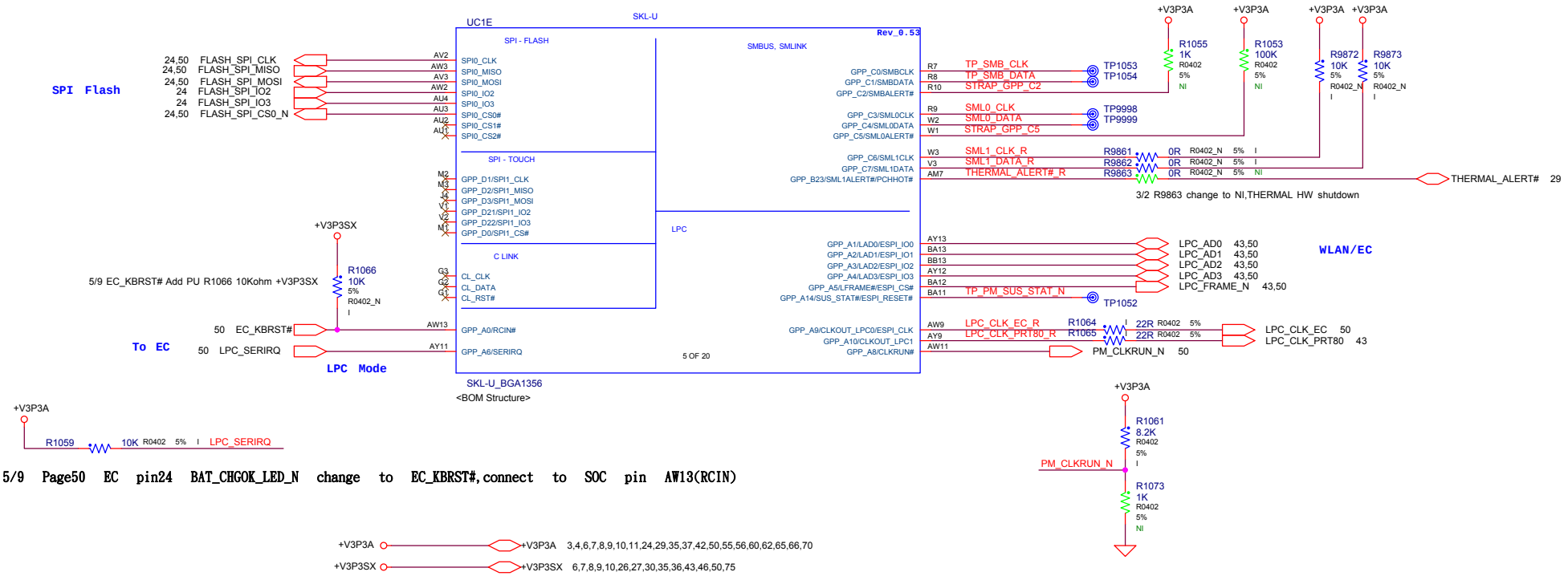
Memory size	4Gb or 8Gb	16Gb	
DRAM M9 pin	RM95,RM96,RM97,RM98 need uninstall RM99,RM100 need install	RM95,RM96,RM97,RM98 need install RM99,RM100 need uninstall	page4,19,20
DRAM E9 pin	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 0 ohm	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 240 ohm	page19,20
SOC RCOMP0	RM3 200 ohm need install	RM3 121 ohm need install	page4

2/2 Add (4Gb 8Gb) & (16Gb) BOM option table



+V3P3A +V3P3A 3,5,6,7,8,9,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70
+V1P2U_VDDQ +V1P2U_VDDQ 10,19,20,21,61

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(2/12)DDR4	Rev: V01
Date: Tuesday, May 23, 2017	Sheet 4 of 81	



5/9 Page50 EC pin24 BAT_CHGOK_LED_N change to EC_KBRST#,connect to SOC pin AW13(RCIN)

SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

SML1ALERT# / PCHHOT#/ GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(3/12)SPI,ESPI,SMB,LPC	Rev: V01
Date: Monday, April 10, 2017	Sheet 5 of 81	

To Enable ME Override

50 ME_Flash_EN — R9848 0R 5% I (R0402_N) — STRAP_HDA_SDO_SOC

Difference with armour
Add EC to enable ME override

5/23 R9848 install,BIOS request

HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

46 HDA_SYNC — RC393 33R R0402 5% I — HDA_SYNC_SOC
46 HDA_BCLK_R — R1086 33R R0402 5% I — HDA_BCLK
46 STRAP_HDA_SDO — RC395 33R R0402 5% I — STRAP_HDA_SDO_SOC
46 HDA_RST_N — RC394 33R R0402 5% I — HDA_RST_N_SOC

+V3P3A — R1054 1K R0402 5% NI

HDA for AUDIO

46 HDA_SDI0

UC1G — SKL-U — Rev_0.53

AUDIO

Signal	Pin
HDA_SYNC_SOC	BA22
HDA_BCLK	AY22
STRAP_HDA_SDO_SOC	BB22
HDA_SDI0	BA21
	AY21
HDA_RST_N_SOC	AW22
	J5
	AY20
	AW20
	AK7
	AK6
	AK9
	AK10
	H5
	D7
	D8
	C8
	AW5

HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR

SDIO/SDXC

Signal	Pin
GPP_G0/SD_CMD	AB11
GPP_G1/SD_DATA0	AB13
GPP_G2/SD_DATA1	AB12
GPP_G3/SD_DATA2	W12
GPP_G4/SD_DATA3	W11
GPP_G5/SD_CD#	W10
GPP_G6/SD_CLK	W8
GPP_G7/SD_WP	W7
GPP_A17/SD_PWR_EN#/ISH_GP7	BA9
GPP_A16/SD_1P8_SEL	BB9
SD_RCOMP	AB7
GPP_F23	AF13

7 OF 20

43 WIFI_DISABLE_N

+V3P3SX — R1052 100K 5% NI R0402

46 HDA_SPKR

1/4 Connect codec

SKL-U_BGA1356
<BOM Structure>

TP_SD_WP — R9864 0R R0402_N 5% NI

Difference with armour
Add 0ohm NI

SDMMC_RCOMP — R1015 200R R0402 1% I

+V3P3A — +V3P3A 3,4,5,7,8,9,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70
+V3P3SX — +V3P3SX 5,7,8,9,10,26,27,30,35,36,43,46,50,75

UC1I — SKL_ULT — Rev_0.53

CSI-2

Signal	Pin
CSI2_DN0	A36
CSI2_DP0	B36
CSI2_DN1	C38
CSI2_DP1	D38
CSI2_DN2	C36
CSI2_DP2	D36
CSI2_DN3	A38
CSI2_DP3	B38
CSI2_DN4	C31
CSI2_DP4	D31
CSI2_DN5	C33
CSI2_DP5	D33
CSI2_DN6	A31
CSI2_DP6	B31
CSI2_DN7	A33
CSI2_DP7	B33
CSI2_DN8	A29
CSI2_DP8	B29
CSI2_DN9	C28
CSI2_DP9	D28
CSI2_DN10	A27
CSI2_DP10	B27
CSI2_DN11	C27
CSI2_DP11	D27

Signal	Pin
CSI2_CLKN0	C37
CSI2_CLKP0	D37
CSI2_CLKN1	C32
CSI2_CLKP1	D32
CSI2_CLKN2	C29
CSI2_CLKP2	D29
CSI2_CLKN3	B26
CSI2_CLKP3	A26
CSI2_COMP	E13
GPP_D4/FLASHTRIG	B7

EMMC

Signal	Pin
GPP_F13/EMMC_DATA0	AP2
GPP_F14/EMMC_DATA1	AP1
GPP_F15/EMMC_DATA2	AP3
GPP_F16/EMMC_DATA3	AN3
GPP_F17/EMMC_DATA4	AN1
GPP_F18/EMMC_DATA5	AN2
GPP_F19/EMMC_DATA6	AM4
GPP_F20/EMMC_DATA7	AM1
GPP_F21/EMMC_RCLK	AM2
GPP_F22/EMMC_CLK	AM3
GPP_F12/EMMC_CMD	AP4
EMMC_RCOMP	AT1

9 OF 20

SKL-U_BGA1356
<BOM Structure>

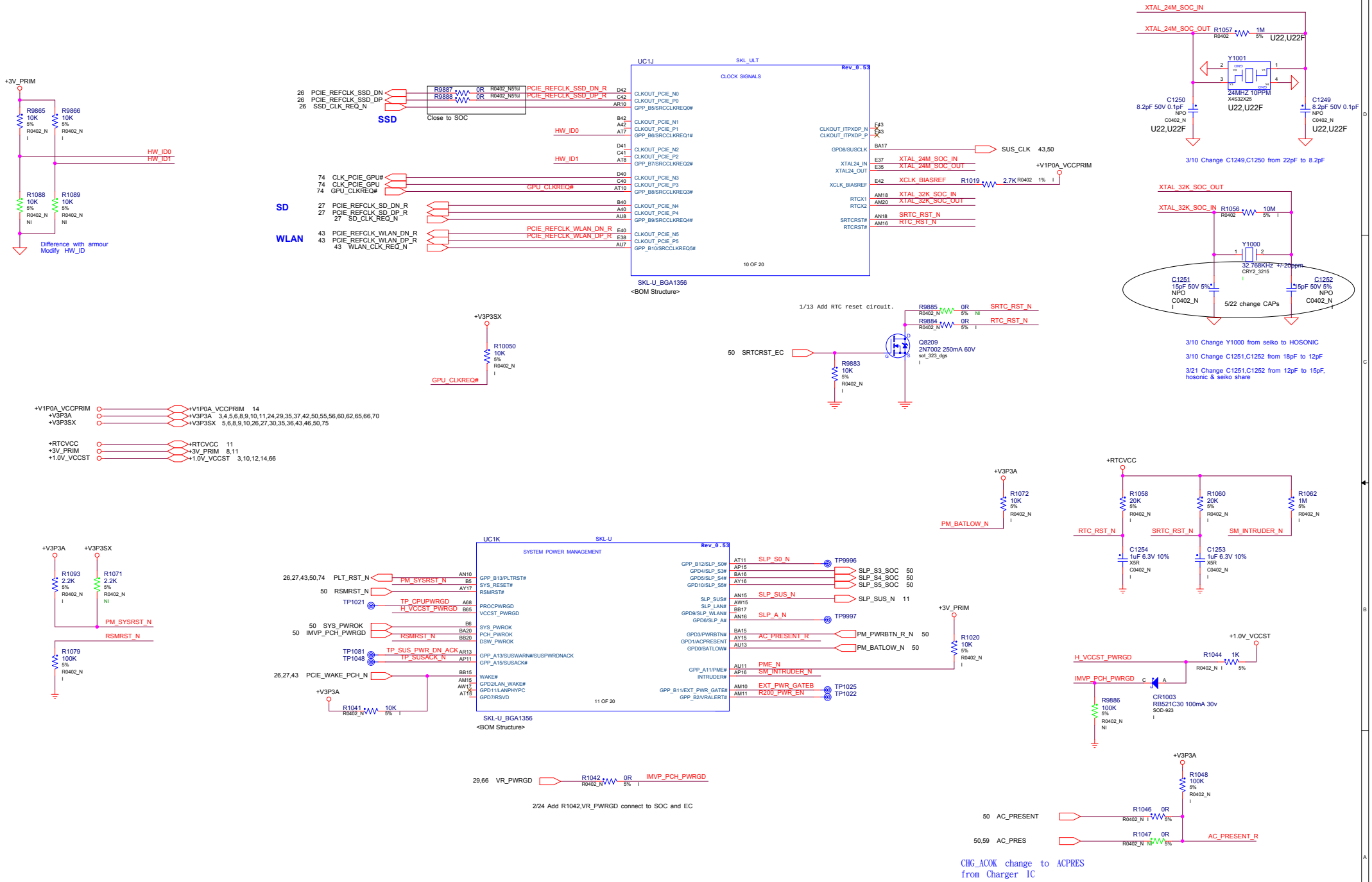
CSI2_COMP — R1013 100R R0402 1% I
CSI2_FLASH_STROBE — TP1061

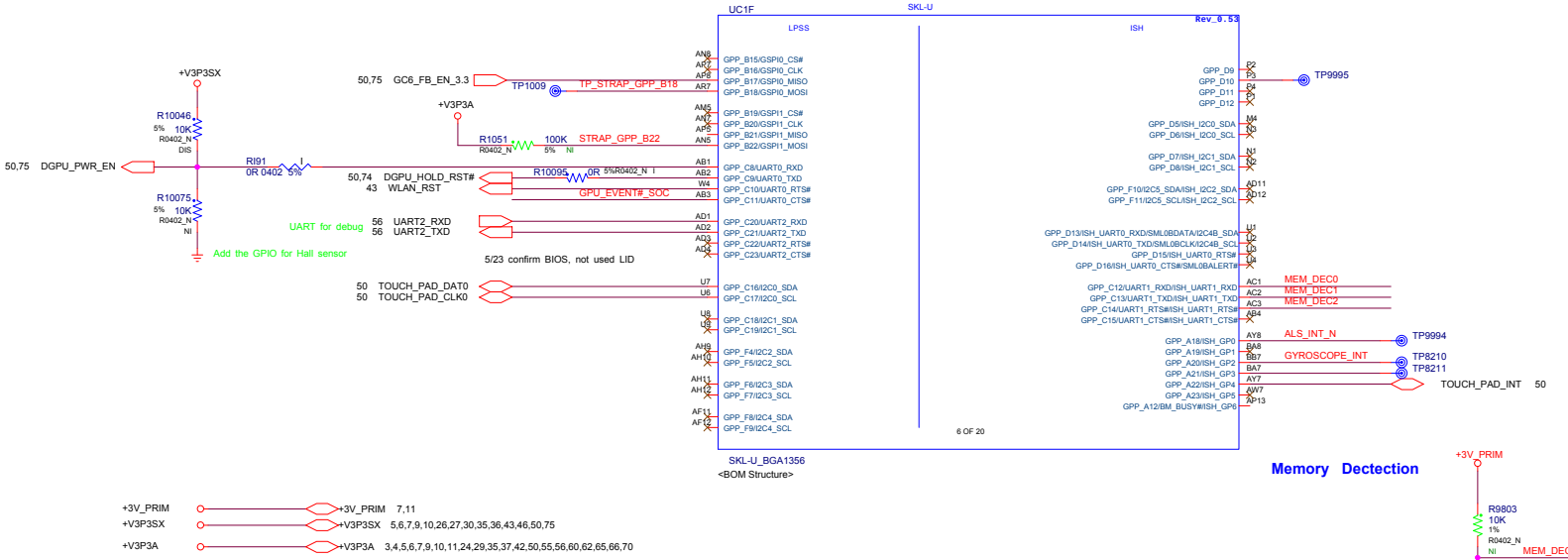
3/18 Add TP1061

EMMC_RCOMP — R1014 200R R0402 1% I

5/10 Del TP1055,TP1056,TP1057,TP1058,TP1059,TP1060,TP1016,TP1017,
MIPI defferential don't test point

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(4/12)HDA,EMMC,SD	Rev: V01
Date: Monday, April 10, 2017	Sheet 6 of 81	


UC1J
SKL_ULT
Rev_0.53
CLOCK SIGNALS
10 OF 20
SKL-U_BGA1356
<BOM Structure>
SSD
SD
WLAN
Close to SOC
Difference with armour
Modify HW_ID
XTAL_24M_SOC_IN
XTAL_24M_SOC_OUT
XTAL_32K_SOC_OUT
XTAL_32K_SOC_IN
3/10 Change C1249,C1250 from 22pF to 8.2pF
3/10 Change Y1000 from seiko to HOSONIC
3/10 Change C1251,C1252 from 18pF to 12pF
3/21 Change C1251,C1252 from 12pF to 15pF, hosonic & seiko share
5/22 change CAPs
1/13 Add RTC reset circuit.
UC1K
SKL-U
Rev_0.53
SYSTEM POWER MANAGEMENT
11 OF 20
SKL-U_BGA1356
<BOM Structure>
2/24 Add R1042,VR_PWRGD connect to SOC and EC
CHG_ACOK change to ACPRES
from Charger IC
Project: 320S-13
Engineer: Jason
Size: Custom
Title: KBL-U(5/12)CLK,GPIO
Rev: V01
Date: Monday, May 22, 2017
Sheet 7 of 81



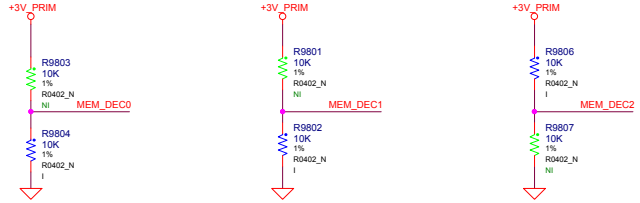
+3V_PRIM — +3V_PRIM 7,11

+V3P3SX — +V3P3SX 5,6,7,9,10,26,27,30,35,36,43,46,50,75

+V3P3A — +V3P3A 3,4,5,6,7,9,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70

75 GPU_EVENT# — DIS SOD_323 BAT54WS D6607 — GPU_EVENT#_SOC

Memory Dectection



	Samsung_4GB	Micron_4GB	Hynix_4GB	Samsung_8GB	Micron_8GB	Hynix_8GB	Samsung_16GB	Micron_16GB
MEM_DEC0	0	1	0	1	0	1	0	1
MEM_DEC1	0	0	1	1	0	0	1	1
MEM_DEC2	0	0	0	0	1	1	1	1

Default

GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Keyparts	Character	Supplier	Description	3NOD PN	Lenovo P/N
Lenovo B/S part sourcing plan					
CPU	Intel® 6th Gen Core™	Intel	i3-6100U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i3-6100U 2.3G/2C/3M intel)	457100266700	SSA0K07374
		Intel	i5-6200U 2.3G/2C/3M (CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i5-6200U 2.3G/2C/3M intel)	457100266800	SSA0K07375
		Intel	i7-6500U 2.5G/2C/4M(CPU 7.5w BGA1356 2 Skylake-U, 6th Gen Intel Core I i7-6500U 2.5G/2C/4M intel)	457100266900	SSA0K07377
DRAM	4Gbx16 DDR4 2400 SDRAM (单颗容量 0.5GB)	Samsung	K4A4G165WE-BCRC (MEMORY DDR4-2400 256Mx16 96FBGA K4A4G165WE-BCRC Samsung SM30L08878)	403670650600	SM30L08878
		Micron(Elpida)	MT40A256M16GE-083E:B		SM30L08871
		Hynix	H5AN4G6NAFR-UHC (MEMORY DDR4 2400 256M x 16 96ball FBGA H5AN4G6NAFR-UHC Hynix SM30L08876)	403670650800	SM30L08876
	8Gbx16 DDR4 2400 SDRAM (单颗容量 1GB)	Samsung	K4A8G165WB-BCRC (MEMORY DDR4-2400 512Mx16 96FBGA K4A8G165WB-BCRC Samsung SM30L08874)	403670650700	SM30L08874
		Micron(Elpida)	MT40A512M16JY-083E:B	403670650900	SM30L08877
		Hynix	H5AN8G6NAFR-UHC (MEMORY DDR4 2400 512M*16 96FBGA MT40A512M16JY-083E:B Micron SM30L08877)		SM30L08875

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(6/12)GPIO	Rev: V01
Date: Tuesday, May 23, 2017	Sheet 8 of 81	

High Speed I/O (HSIO) Lane Multiplexing in SKL U

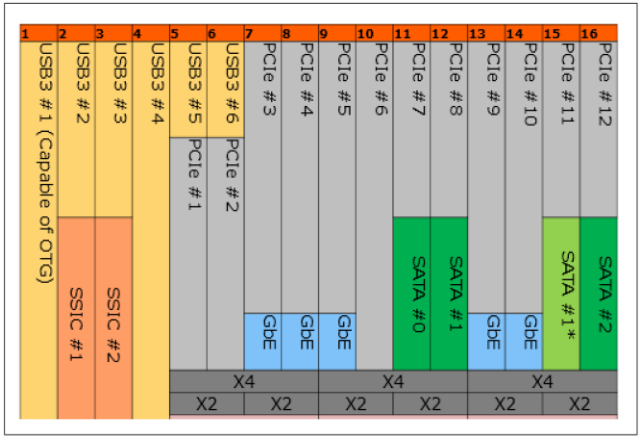


Table 1-3. PCH HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe*	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe* / USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

+V3P3A
+V3P3SX

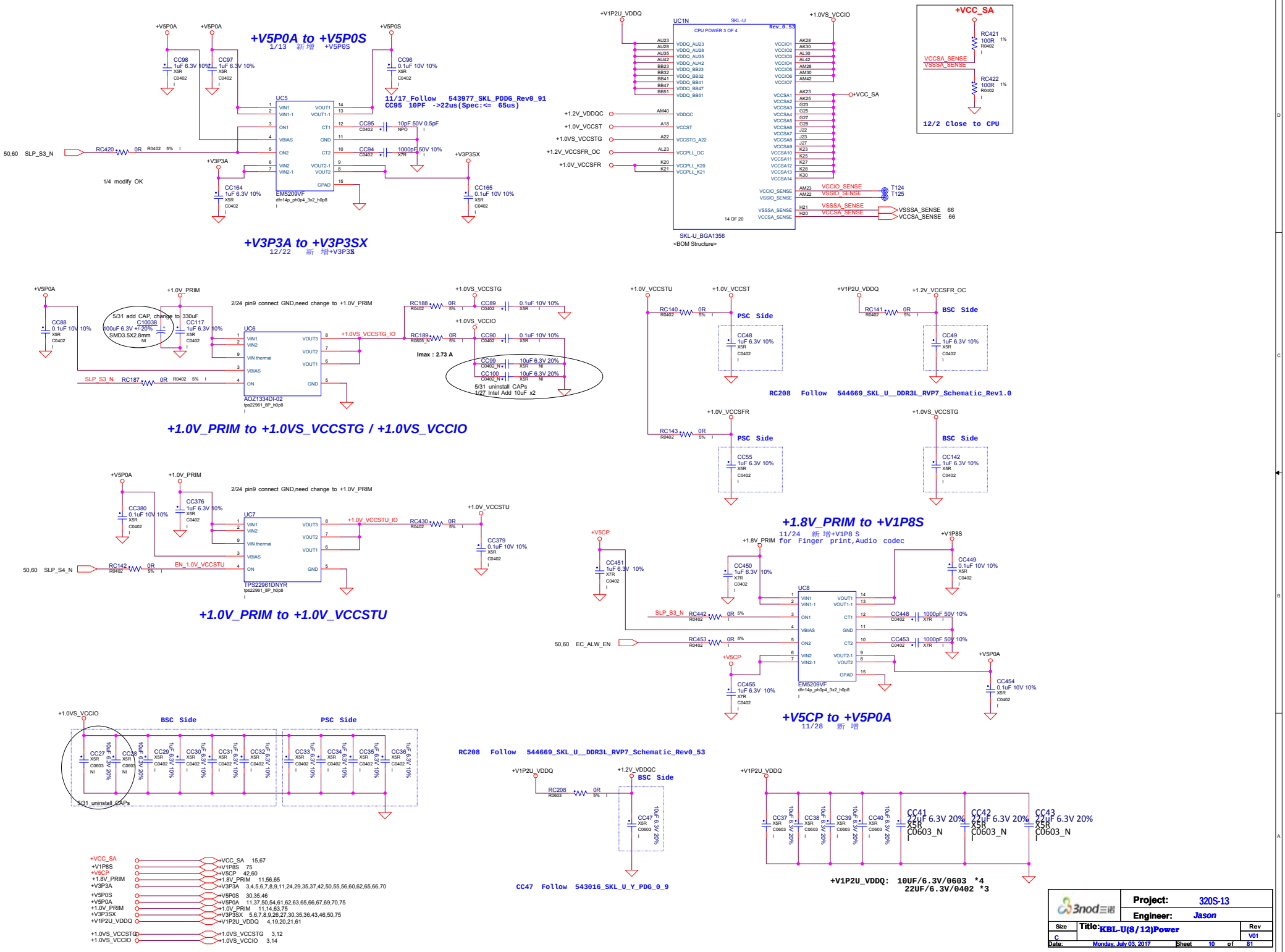
+V3P3A 3,4,5,6,7,8,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70
+V3P3SX 5,6,7,8,10,26,27,30,35,36,43,46,50,75

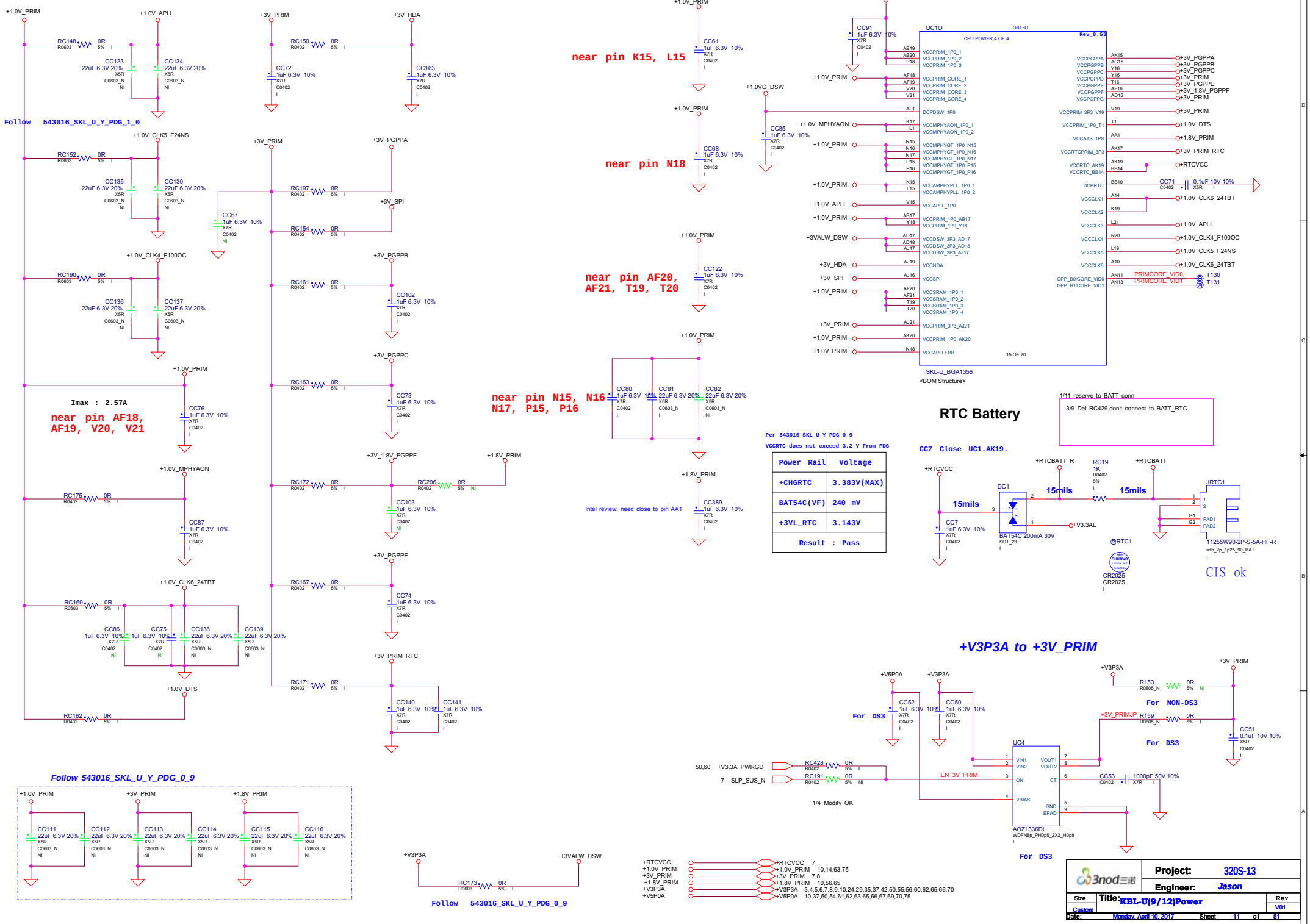
+V3P3A
R9882 10K 5% R0402_N I
USB2_P2_WP3_OC_N
1/7 Add PU +V3P3A

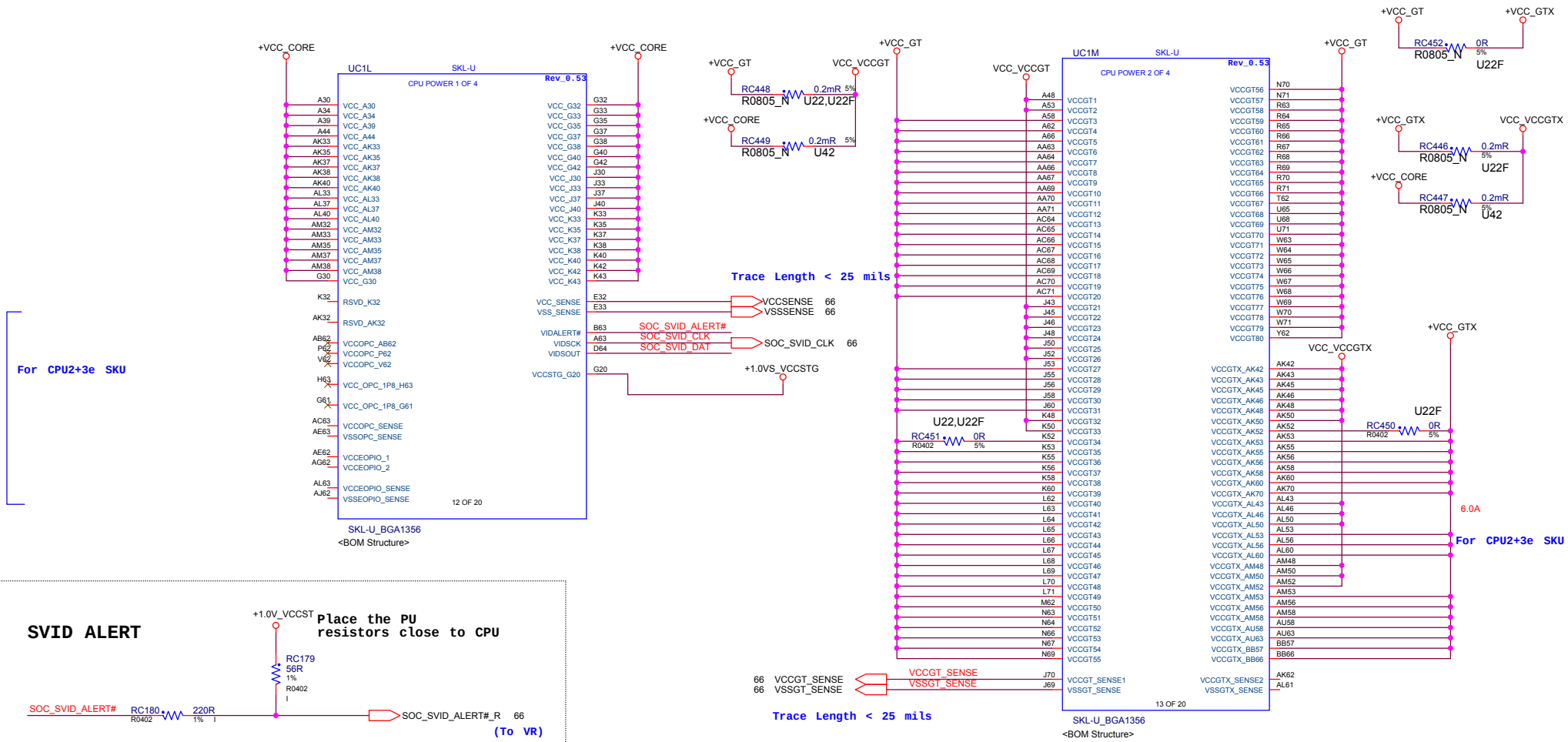
+V3P3SX
Difference with armour
R1050 install,R1087 uninstall
R1087 100K 5% R0402_N NI
SSD_SATA_PCIE_DET_N
R1050 10K 5% R0402_N I

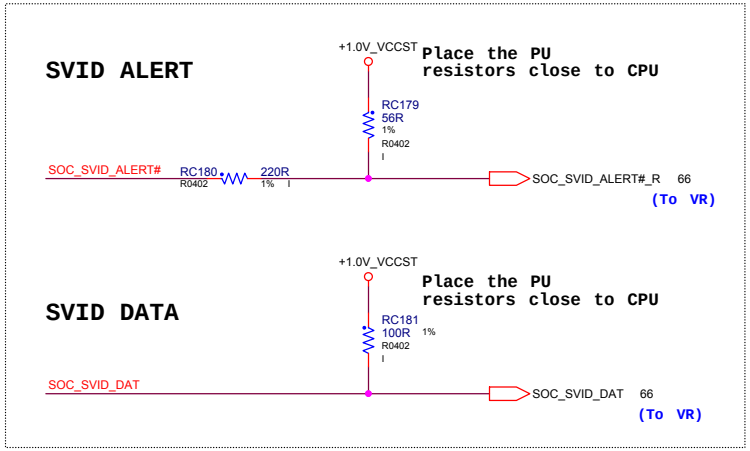
NOTE:
USE FITC TO ALLOW SELECTION OF
PCIE VS SATA BASED ON STRAPPING:
GPP_E_2 FOR SATA2/PCIE:
1 - SATA2, 0 - PCIE P9,P10,P11,P12

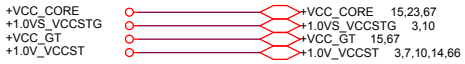
3nod三诺	Project: 320S-13		
	Engineer: Jason		
Size: Custom	Title: KBL-U(7/12)PCIE,USB,SATA		Rev: V01
Date: Monday, April 10, 2017	Sheet 9 of 81		

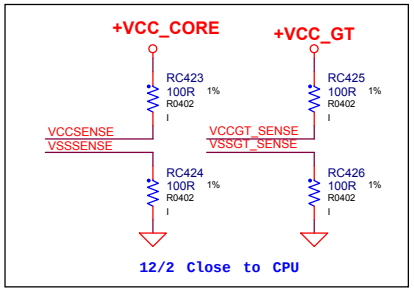

+V5P0A to +V5P0S
1/13 新增 +V5P0S
11/17_Follow 543977_SKL_PDDG_Rev0_91
CC95 10PF ->22us(Spec:<= 65us)
UC5
EM5209VF
+V3P3A to +V3P3SX
12/22 新 增+V3P3S
UC1N
SKL-U
CPU POWER 3 OF 4
Rev_0.53
SKL-U_BGA1356
<BOM Structure>
+VCC_SA
12/2 Close to CPU
+1.0V_PRIM to +1.0VS_VCCSTG / +1.0VS_VCCIO
2/24 pin9 connect GND,need change to +1.0V_PRIM
5/31 add CAP, change to 330uF
AOZ1334DI-02
Imax : 2.73 A
5/31 uninstall CAPs
1/27 Intel Add 10uF x2
PSC Side
BSC Side
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev1.0
+1.8V_PRIM to +V1P8S
11/24 新 增+V1P8 S
for Finger print,Audio codec
+1.0V_PRIM to +1.0V_VCCSTU
TPS22961DNYR
+V5CP to +V5P0A
11/28 新 增
5/31_uninstall_CAPs
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53
CC47 Follow 543016_SKL_U_Y_PDG_0_9
+V1P2U_VDDQ: 10UF/6.3V/0603 *4
22UF/6.3V/0402 *3
Project: 320S-13
Engineer: Jason
Title: KBL-U(8/12)Power
Size C
Rev V01
Date: Monday, July 03, 2017
Sheet 10 of 81


Follow 543016_SKL_U_Y_PDG_1_0
Imax : 2.57A
near pin AF18, AF19, V20, V21
near pin K15, L15
near pin N18
near pin AF20, AF21, T19, T20
near pin N15, N16, N17, P15, P16
Intel review: need close to pin AA1
Per 543016_SKL_U_Y_PDG_0_9
VCCRTC does not exceed 3.2 V From PDG
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
UC1O
SKL-U
CPU POWER 4 OF 4
Rev_0.53
15 OF 20
SKL-U_BGA1356
<BOM Structure>
RTC Battery
1/11 reserve to BATT conn
3/9 Del RC429,don't connect to BATT_RTC
CC7 Close UC1.AK19.
BAT54C 200mA 30V
T1255W90-2P-S-5A-HF-R
CR2025
CIS ok
+V3P3A to +3V_PRIM
For DS3
For NON-DS3
AOZ1336DI
Follow 543016_SKL_U_Y_PDG_0_9
Project: 320S-13
Engineer: Jason
Title: KBL-U(9/12)Power
Date: Monday, April 10, 2017
Sheet 11 of 81







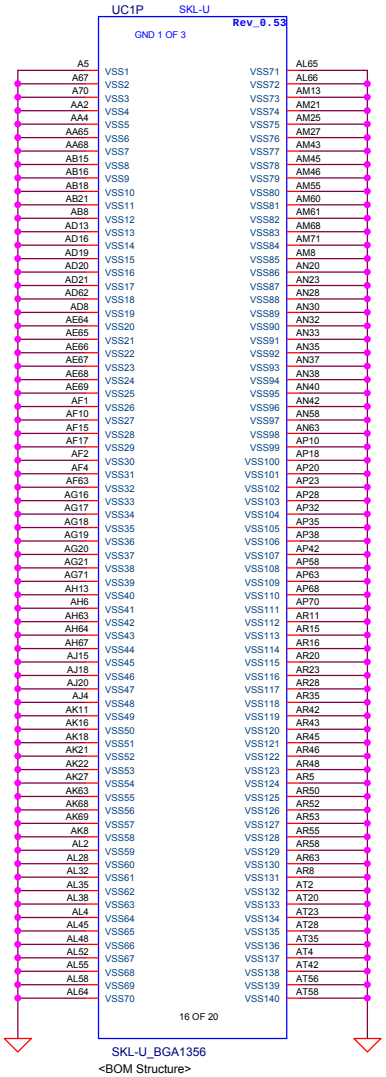


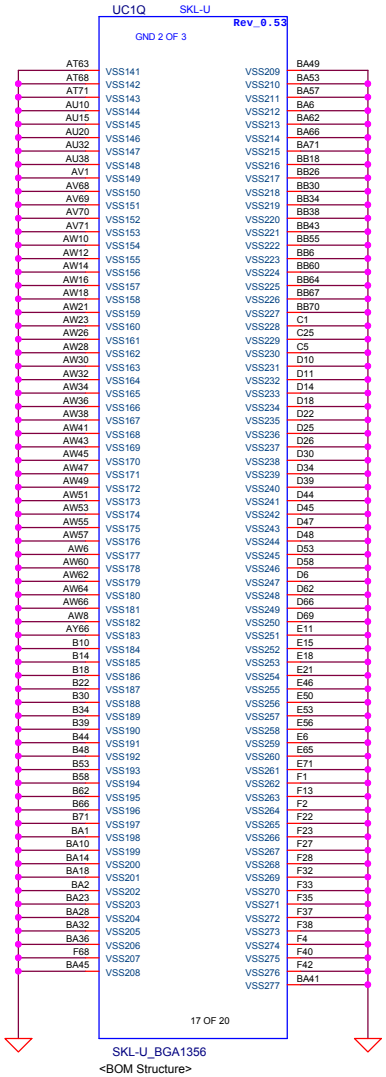
Package Sensing Recommendations

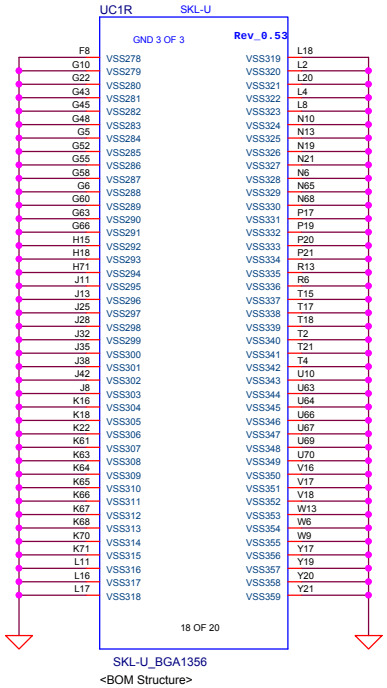
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{GTx}_SENSE / Vss_{GTx}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

Note: [1] Does not apply when rails are merged.

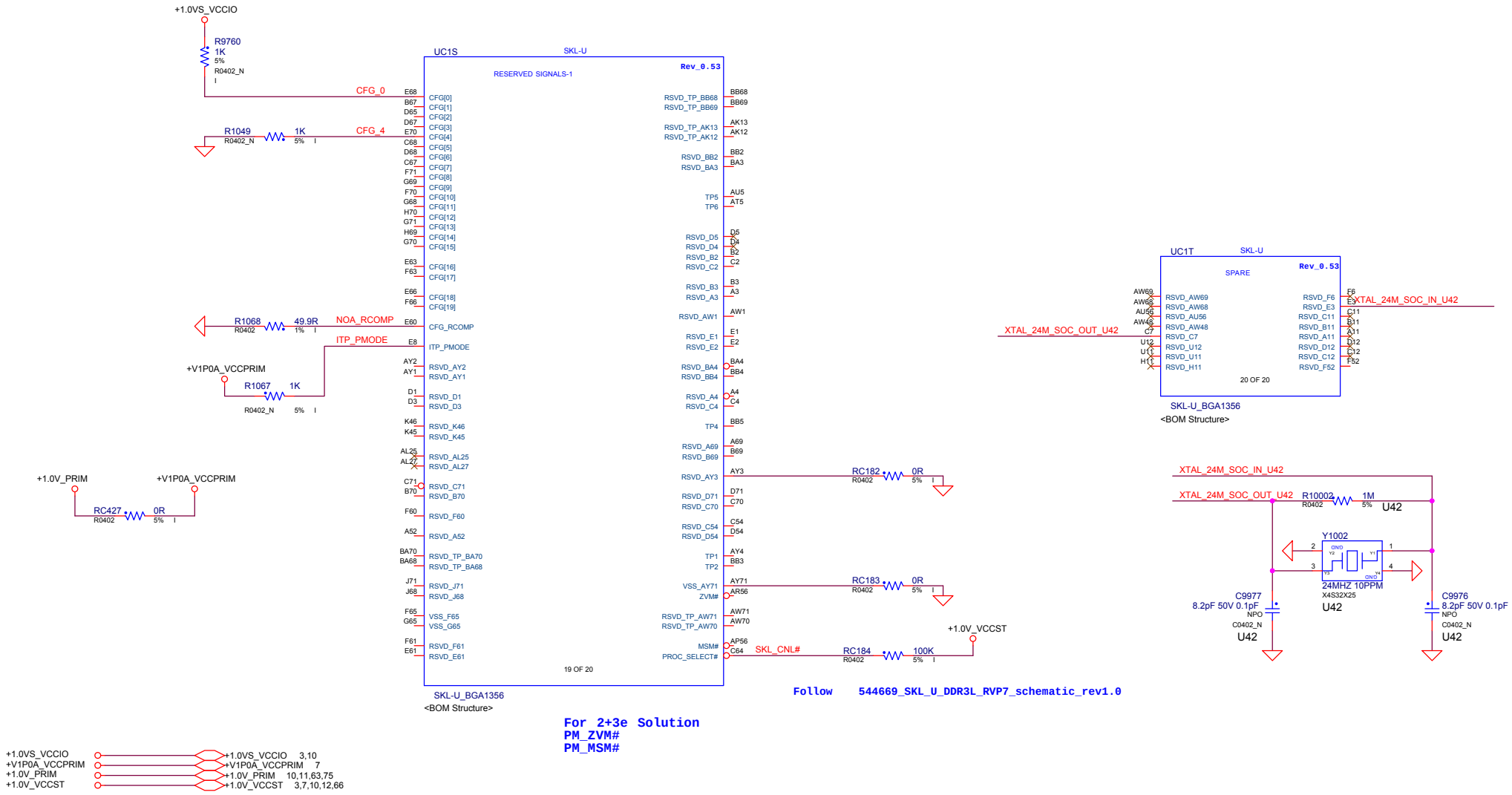
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(10/12)Power,SVID	Rev: V01
Date: Monday, April 10, 2017	Sheet 12 of 81	







3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(11/12)GND	Rev: V01
Date: Monday, April 10, 2017	Sheet 13 of 81	

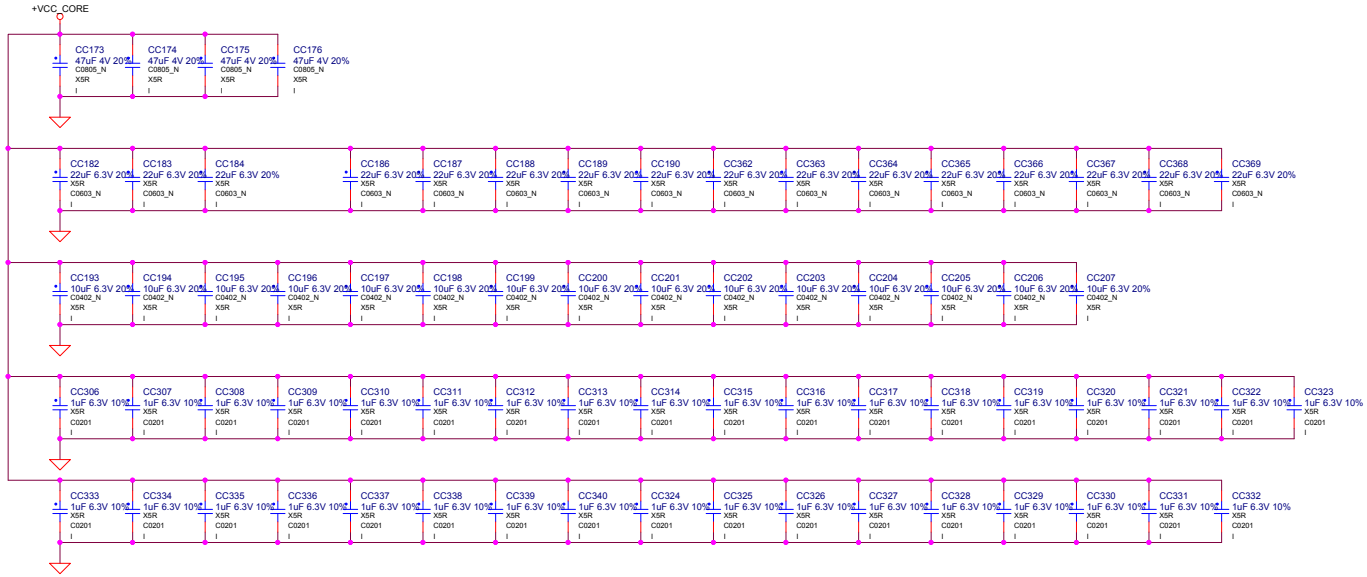


Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

For 2+3e Solution
PM_ZVM#
PM_MSM#

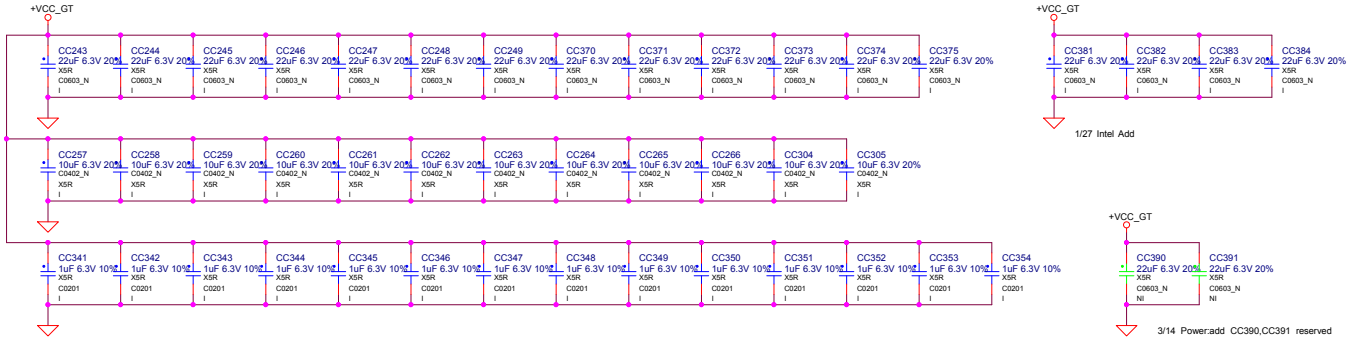
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: KBL-U(12/12)RSVD	Rev: V01
Date: Monday, April 10, 2017	Sheet 14 of 81	



12/30 check PDG
& 220uF pull power side

+VCC_CORE
47uF x8 change 47uF x4
22uF x9 cgange 22uF x17
10uF x15
1uF x35

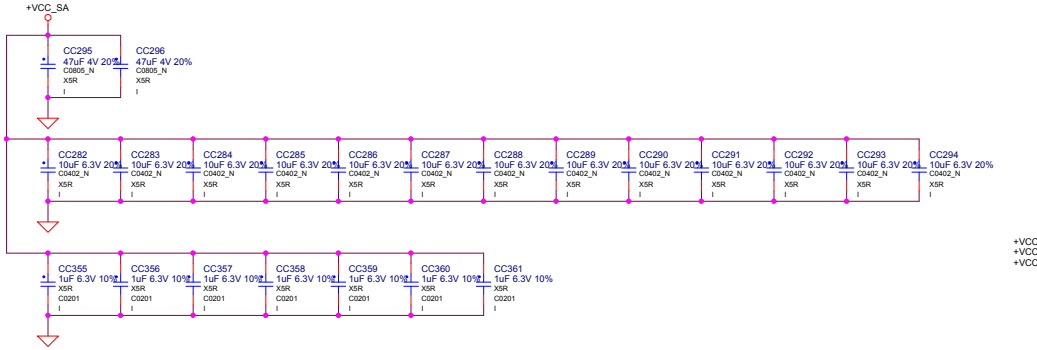


1/27 Intel Add

3/14 Power:add CC390,CC391 reserved

12/30 check PDG
& 220uF pull power side

+VCC_GT
47uF x3 change 47uF x0
22uF x7 cgange 22uF x13
10uF x12
1uF x14



+VCC_SA
47uF x2
10uF x13
1uF x7

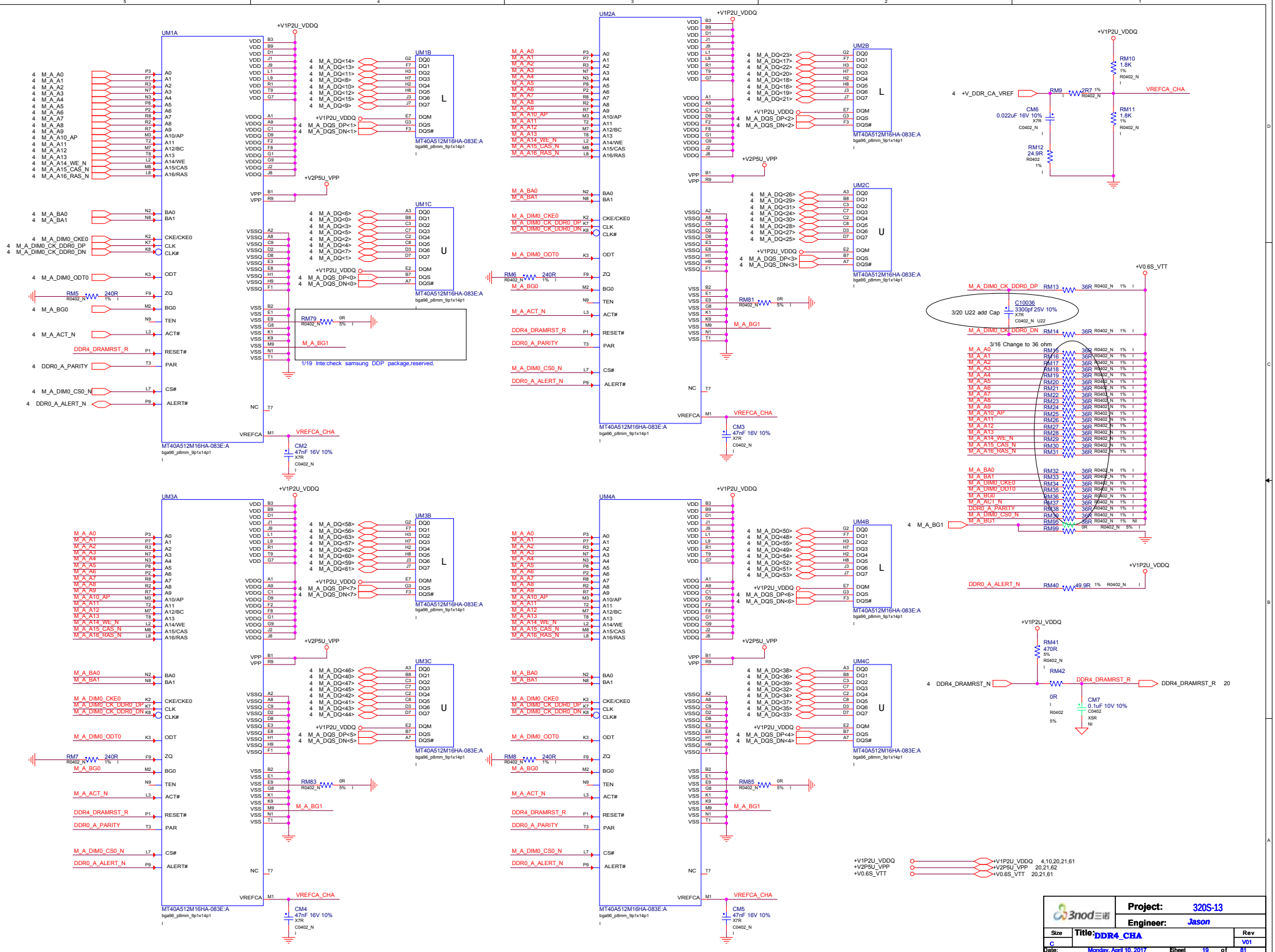
12/30 check PDG

3nod三诺	Project: 320S-13		
	Engineer: Jason		
Size C	Title: SOC (DECOUPLING)		Rev V01
Date: Monday, May 22, 2017	Sheet 15 of 81		

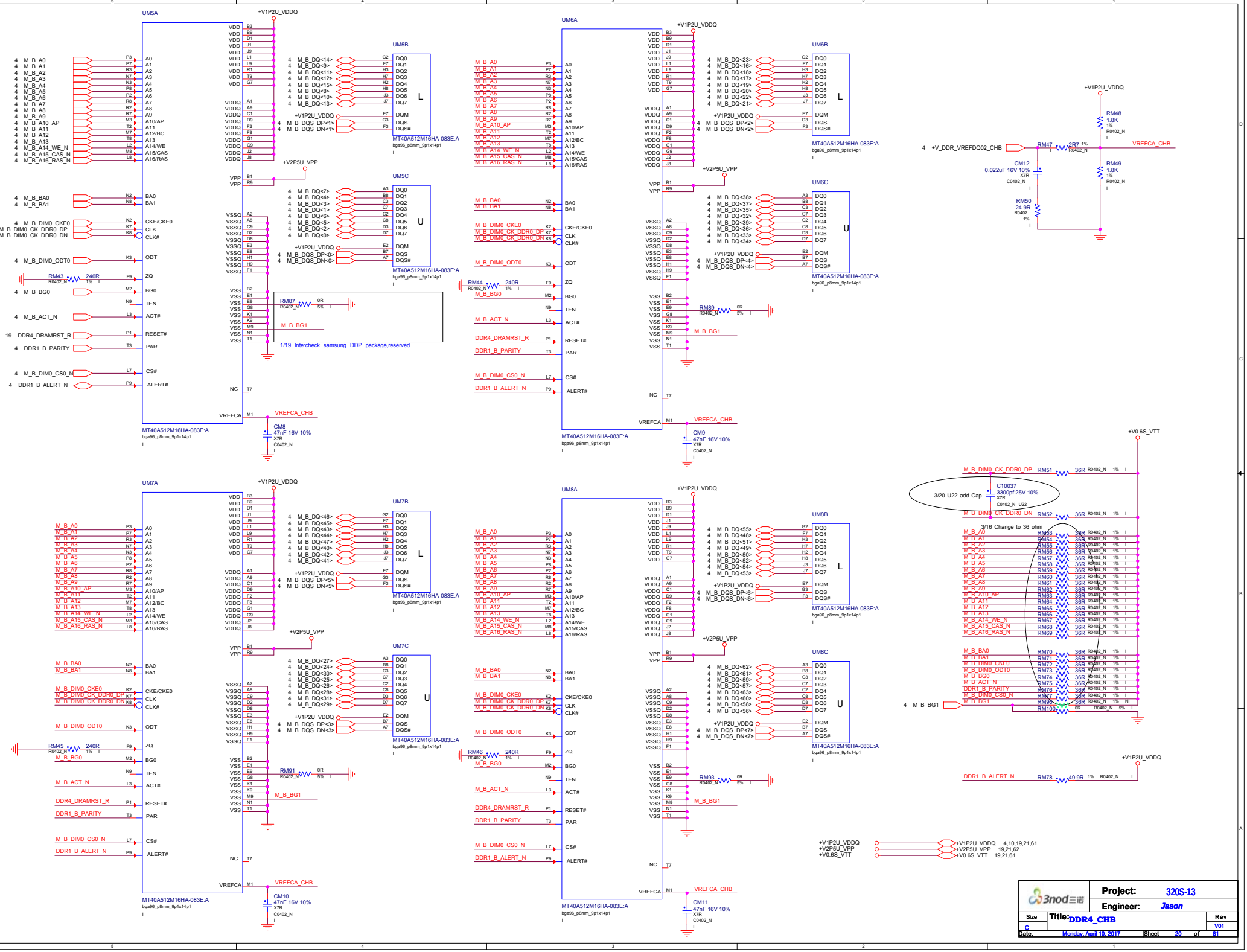
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size B	Title: NA	Rev V01
Date: Monday, April 10, 2017	Sheet 16 of 81	

3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size B	Title: NA	Rev V01
Date: Monday, April 10, 2017	Sheet 17 of 81	

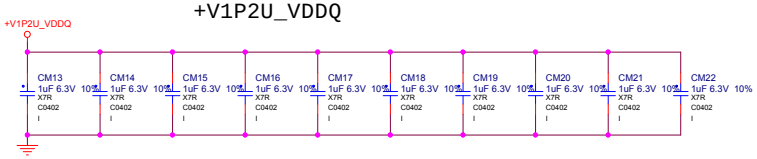
3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 18 of 81	

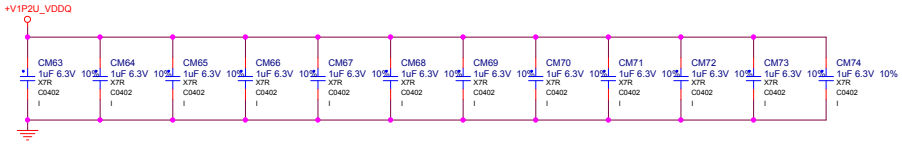


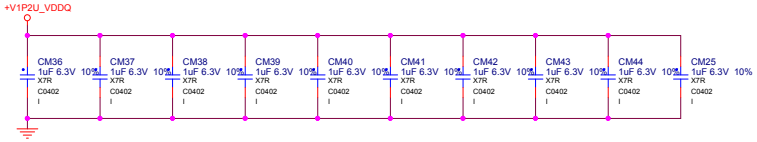
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size C	Title: DDR4_CHA	Rev V01
Date: Monday, April 10, 2017	Sheet 19 of 81	


UM5A
UM5B
UM5C
UM6A
UM6B
UM6C
UM7A
UM7B
UM7C
UM8A
UM8B
UM8C
MT40A512M16HA-083E:A
bga96_p8mm_9p1x14p1
+V1P2U_VDDQ
+V2P5U_VPP
+V0.6S_VTT
VREFCA_CHB
CM8 47nF 16V 10% X7R C0402_N
CM9 47nF 16V 10% X7R C0402_N
CM10 47nF 16V 10% X7R C0402_N
CM11 47nF 16V 10% X7R C0402_N
RM43 240R R0402_N 1%
RM44 240R R0402_N 1%
RM45 240R R0402_N 1%
RM46 240R R0402_N 1%
RM87 0R R0402_N 5%
RM89 0R R0402_N 5%
RM91 0R R0402_N 5%
RM93 0R R0402_N 5%
M_B_BG1
1/19 Inte:check samsung DDP package,reserved.
RM48 1.8K 1% R0402_N
RM49 1.8K 1% R0402_N
RM47 2R7 1% R0402_N
RM50 24.9R 1% R0402_N
CM12 0.022uF 16V 10% X7R C0402_N
4 +V_DDR_VREFDQ02_CHB
3/20 U22 add Cap
C10037 3300pf 25V 10% X7R C0402_N U22
3/16 Change to 36 ohm
RM51 36R R0402_N 1%
RM52 36R R0402_N 1%
RM78 49.9R 1% R0402_N
RM100 0R R0402_N 5%
+V1P2U_VDDQ 4,10,19,21,61
+V2P5U_VPP 19,21,62
+V0.6S_VTT 19,21,61
Project: 320S-13
Engineer: Jason
Size C
Title: DDR4_CHB
Rev V01
Date: Monday, April 10, 2017
Sheet 20 of 81

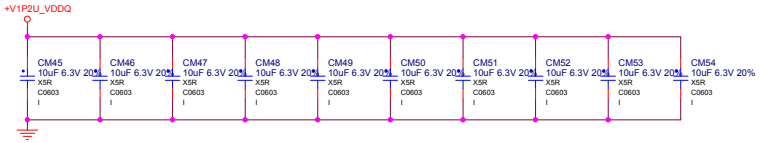
+V1P2U_VDDQ







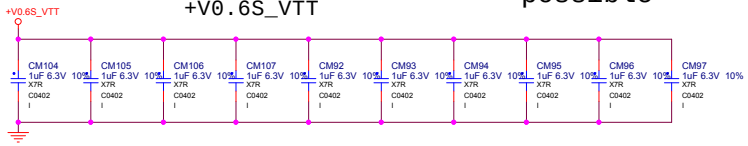
1uF:4 as near each x16 DRAM device as possible

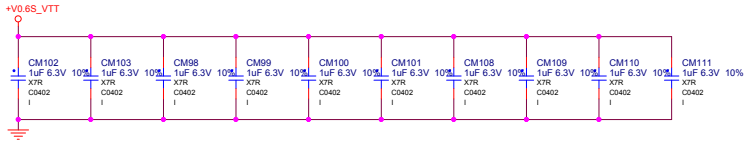


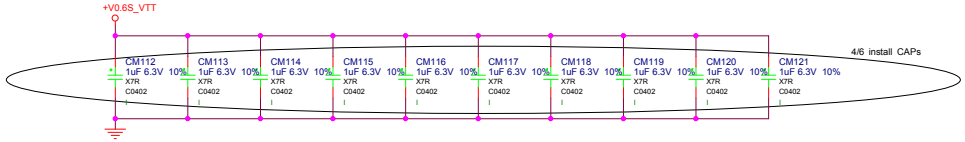
10uF:Distributed around the DRAM devices

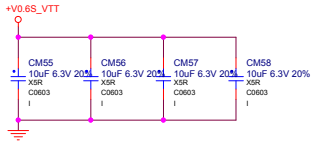
1uF:2 as near each x20 DRAM device as possible

+V0.6S_VTT

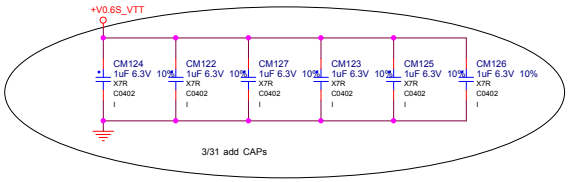




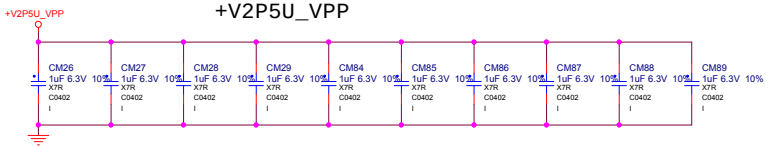


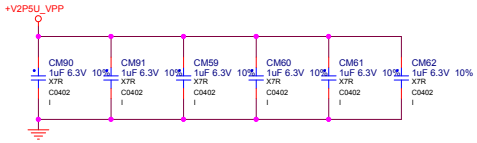


10uF:Distributed around the DRAM devices

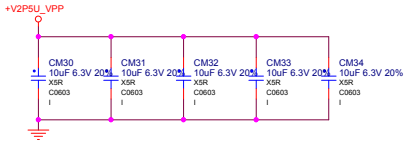


+V2P5U_VPP





1uF:2 as near each x16 DRAM device as possible



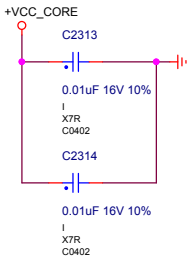
10uF:Distributed around the DRAM devices

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size C	Title: DDR4 Decoupling	Rev V01
Date: Monday, April 10, 2017	Sheet 21 of 81	

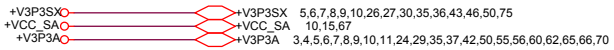
3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 22 of 81	

RF Solution

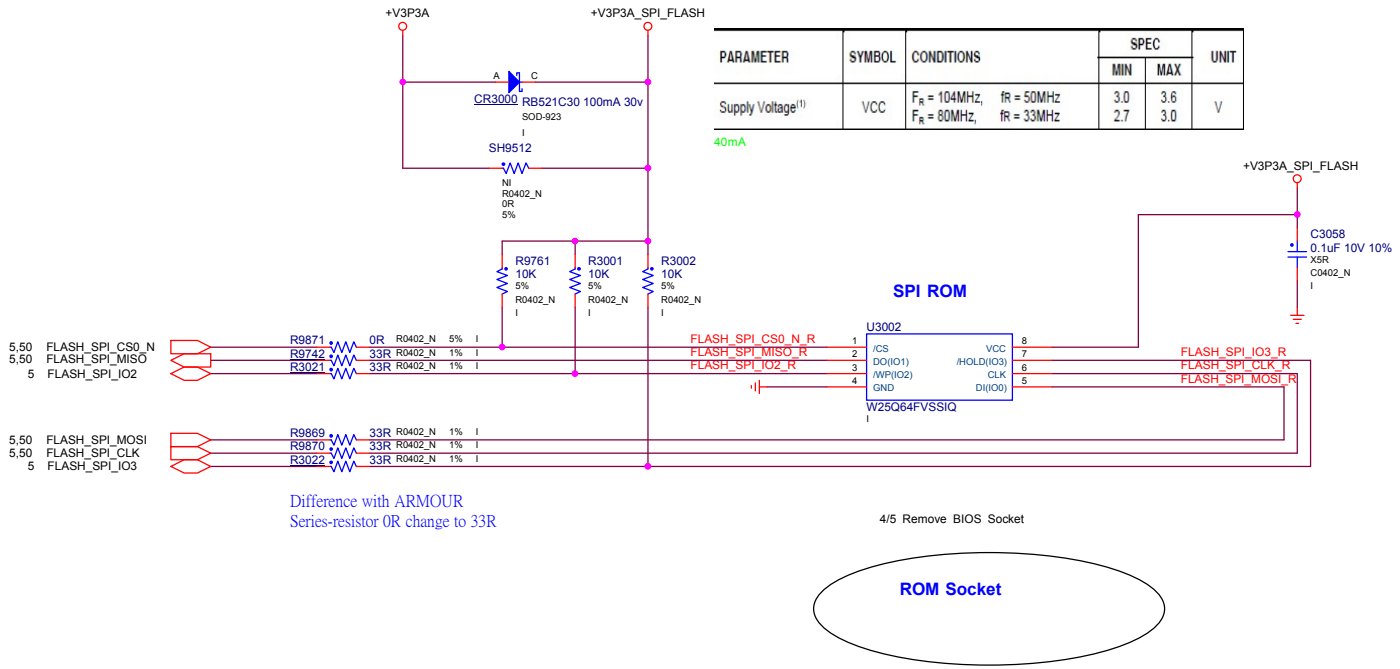
Cross Moat Cap.



EMC Solution



3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: **RF / EMC Solution**	Rev: V01
Date: Monday, April 10, 2017	Sheet 23 of 81	



PARAMETER	SYMBOL	CONDITIONS	SPEC MIN	SPEC MAX	UNIT
Supply Voltage(1)	VCC	F_R = 104MHz, fR = 50MHz F_R = 80MHz, fR = 33MHz	3.0 2.7	3.6 3.0	V

40mA

Difference with ARMOUR
Series-resistor 0R change to 33R

4/5 Remove BIOS Socket

ROM Socket

2/24 SIV:Delet ROM Socket @U3002

+V3P3A +V3P3A 3,4,5,6,7,8,9,10,11,29,35,37,42,50,55,56,60,62,65,66,70

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: SYSTEM FLASH	Rev: V01
Date: Monday, April 10, 2017	Sheet 24 of 81	

INTERNAL ONLY

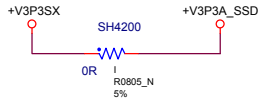
BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:52 2015

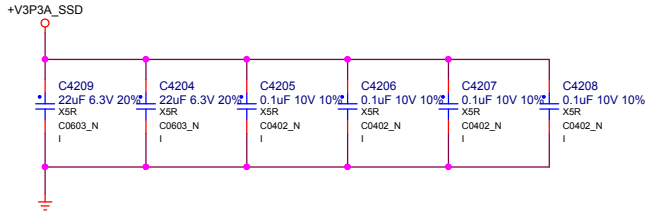
3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 25 of 81	

M.2 SSD Module

1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD

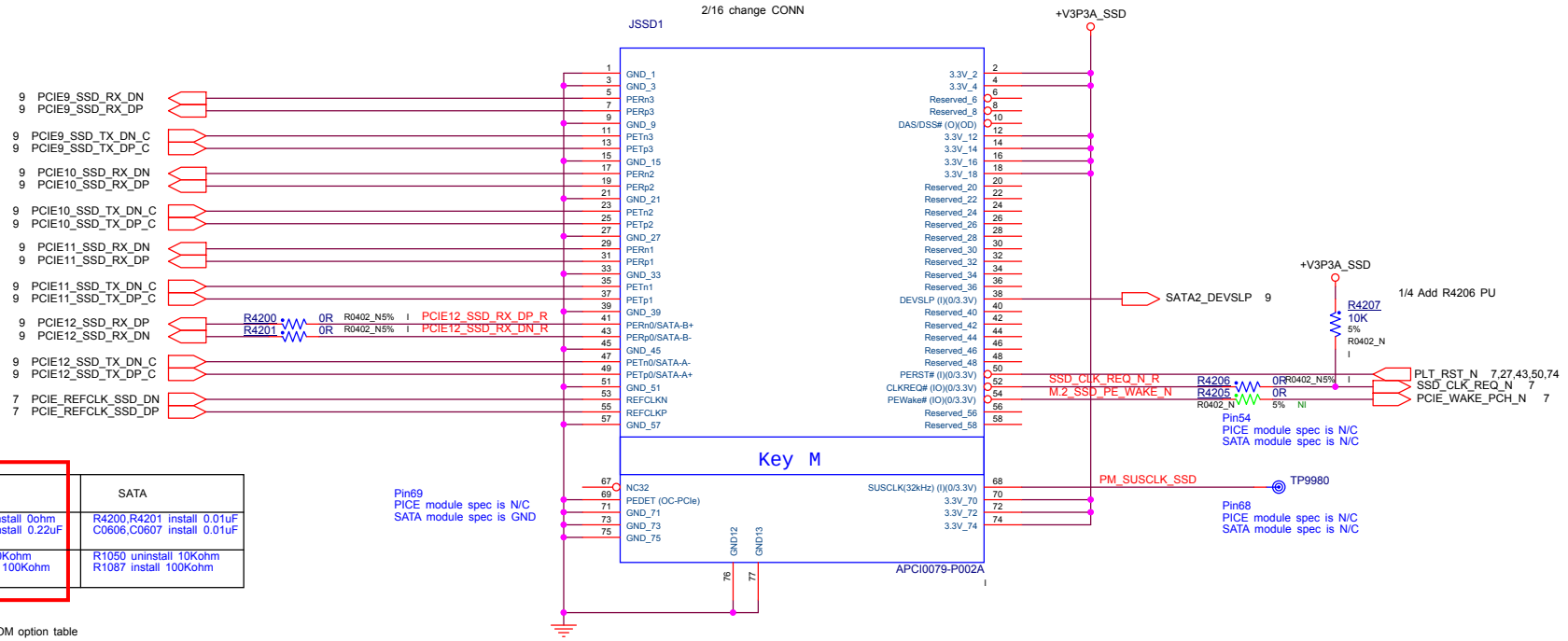


Change SH4200 0805 shunt to resistor



CIS ok

2/16 change CONN



PCIE12 RX follow intel CRB

Difference with armour
SSD interface SATA change to PCIE
If install SATA CARD,R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF

Pin69
PICE module spec is N/C
SATA module spec is GND

Pin54
PICE module spec is N/C
SATA module spec is N/C

Pin68
PICE module spec is N/C
SATA module spec is N/C

NGFF SSD module interface	PCIE	SATA
Reference	R4200,R4201 install 0ohm C0606,C0607 install 0.22uF	R4200,R4201 install 0.01uF C0606,C0607 install 0.01uF
Detect pin	R1050 install 10Kohm R1087 uninstall 100Kohm	R1050 uninstall 10Kohm R1087 install 100Kohm

Default

3/16 Add SSD(PCIE or SATA) BOM option table

Co-lay PCIE12 RX,reserved R4202,R4203
please close to R4200,R4201

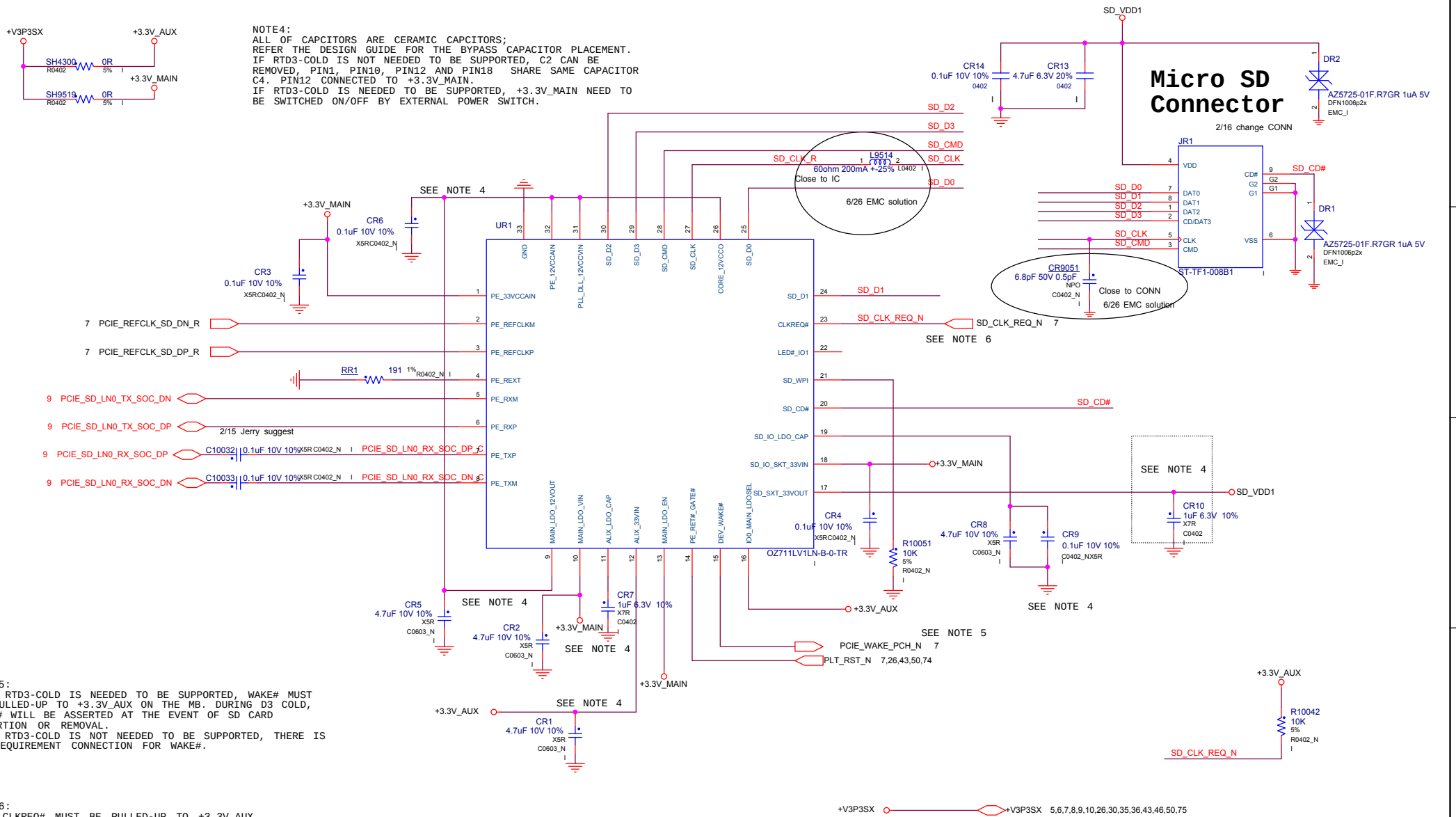
+V3P3SX +V3P3SX 5,6,7,8,9,10,27,30,35,36,43,46,50,75

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.26
Wed Jun 03 11:22:52 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: PCIE SSD MODULE	Rev: V01
Date: Monday, April 10, 2017	Sheet 26 of 81	

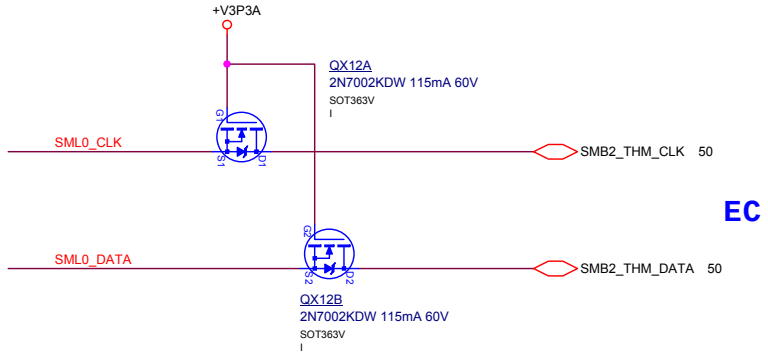

+V3P3SX
+3.3V_AUX
SH4300 0R R0402 5%
+3.3V_MAIN
SH9519 0R R0402 5%
NOTE4:
ALL OF CAPCITORS ARE CERAMIC CAPCITORS;
REFER THE DESIGN GUIDE FOR THE BYPASS CAPACITOR PLACEMENT.
IF RTD3-COLD IS NOT NEEDED TO BE SUPPORTED, C2 CAN BE REMOVED, PIN1, PIN10, PIN12 AND PIN18 SHARE SAME CAPACITOR C4. PIN12 CONNECTED TO +3.3V_MAIN.
IF RTD3-COLD IS NEEDED TO BE SUPPORTED, +3.3V_MAIN NEED TO BE SWITCHED ON/OFF BY EXTERNAL POWER SWITCH.
SD_VDD1
CR14 0.1uF 10V 10% 0402
CR13 4.7uF 6.3V 20% 0402
Micro SD Connector
2/16 change CONN
DR2
AZ5725-01F.R7GR 1uA 5V
DFN1006p2x
EMC_I
JR1
VDD
DAT0
DAT1
DAT2
CD/DAT3
CLK
CMD
CD#
G2
G1
VSS
ST-TF1-008B1
SD_CD#
DR1
AZ5725-01F.R7GR 1uA 5V
DFN1006p2x
EMC_I
SD_D2
SD_D3
SD_CMD
SD_CLK
SD_D0
SD_CLK_R
L9514
60ohm 200mA +-25% L0402
Close to IC
6/26 EMC solution
SEE NOTE 4
+3.3V_MAIN
CR6 0.1uF 10V 10% X5RC0402_N
UR1
GND
PE_12VCCAIN
PLL_DLL_12VCCVIN
SD_D2
SD_D3
SD_CMD
SD_CLK
CORE_12VCCO
SD_D0
CR3 0.1uF 10V 10% X5RC0402_N
PE_33VCCAIN
PE_REFCLKM
PE_REFCLKP
PE_REXT
PE_RXM
PE_RXP
PE_TXP
PE_TXM
SD_D1
CLKREQ#
LED#_IO1
SD_WPI
SD_CD#
SD_IO_LDO_CAP
SD_IO_SKT_33VIN
SD_SXT_33VOUT
MAIN_LDO_12VOUT
MAIN_LDO_VIN
AUX_LDO_CAP
AUX_33VIN
MAIN_LDO_EN
PE_RET#_GATE#
DEV_WAKE#
IO0_MAIN_LDO_SEL
OZ711LV1LN-B-0-TR
7 PCIE_REFCLK_SD_DN_R
7 PCIE_REFCLK_SD_DP_R
RR1 191 1% R0402_N
9 PCIE_SD_LN0_TX_SOC_DN
9 PCIE_SD_LN0_TX_SOC_DP
2/15 Jerry suggest
9 PCIE_SD_LN0_RX_SOC_DP
C10032 0.1uF 10V 10% X5R C0402_N
PCIE_SD_LN0_RX_SOC_DP_C
9 PCIE_SD_LN0_RX_SOC_DN
C10033 0.1uF 10V 10% X5R C0402_N
PCIE_SD_LN0_RX_SOC_DN_C
SD_CLK_REQ_N 7
SEE NOTE 6
+3.3V_MAIN
SD_VDD1
CR10 1uF 6.3V 10% X7R C0402
CR4 0.1uF 10V 10% X5RC0402_N
R10051 10K 5% R0402_N
CR8 4.7uF 10V 10% X5R C0603_N
CR9 0.1uF 10V 10% C0402_NX5R
+3.3V_AUX
CR5 4.7uF 10V 10% X5R C0603_N
CR2 4.7uF 10V 10% X5R C0603_N
CR7 1uF 6.3V 10% X7R C0402
SEE NOTE 5
PCIE_WAKE_PCH_N 7
PLT_RST_N 7,26,43,50,74
+3.3V_AUX
CR1 4.7uF 10V 10% X5R C0603_N
R10042 10K 5% R0402_N
SD_CLK_REQ_N
NOTE5:
1.IF RTD3-COLD IS NEEDED TO BE SUPPORTED, WAKE# MUST BE PULLED-UP TO +3.3V_AUX ON THE MB. DURING D3 COLD, WAKE# WILL BE ASSERTED AT THE EVENT OF SD CARD INSERTION OR REMOVAL.
2.IF RTD3-COLD IS NOT NEEDED TO BE SUPPORTED, THERE IS NO REQUIREMENT CONNECTION FOR WAKE#.
NOTE6:
1.PE_CLKREQ# MUST BE PULLED-UP TO +3.3V_AUX ON THE MB.
2.THE TX/RX/REFCLK/PE_CLKREQ# ARE GROUP SIGNALS, AND EACH PCIE PORT HAS EACH SIGNALS COMBINATION.
PLEASE CONFIRM CHIPSET VENDOR WHICH SIGNALS ARE SAME GROUP, AND CONNECT THOSE GROUP SIGNALS TO OZ711LV1LN.
NOTE3:
TERMINAL 33 (GND) IS THE EXPOSED PAD ON THE BOTTOM OF PACKAGE AND MUST BE SOLDERED TO GND OF PCB.
+V3P3SX
+V3P3SX 5,6,7,8,9,10,26,30,35,36,43,46,50,75
INTERNAL ONLY
BPAGE DRAWING
apl_ff.s
Fri May 27 06:47:20 2016
3nod三诺
Project: 320S-13
Engineer: Jason
Size Custom
Title: <SD CARD>
Rev V01
Date: Monday, June 26, 2017
Sheet 27 of 81

INTERNAL ONLY

BPAGE DRAWING

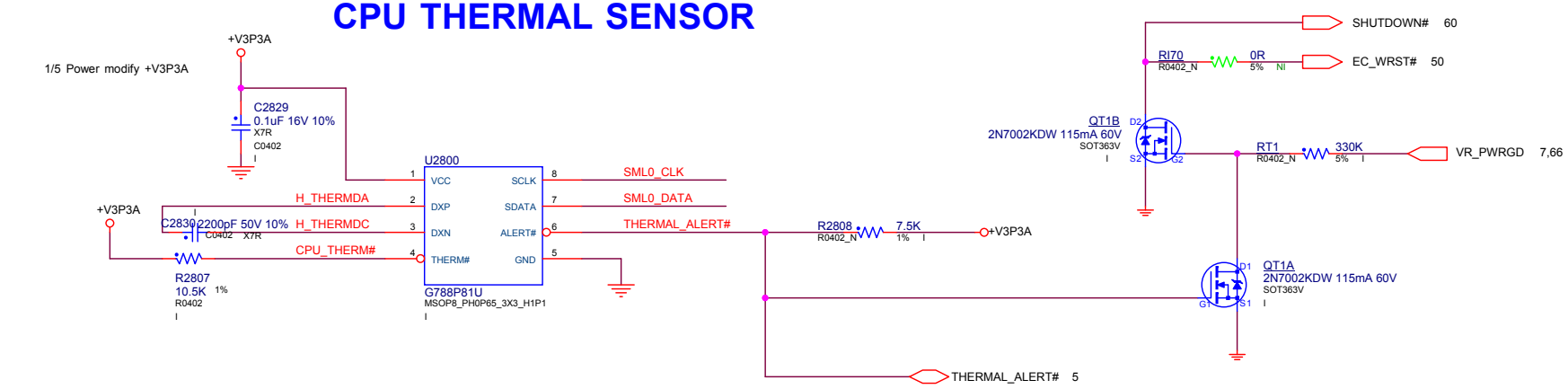
sky_y_mrd.GND
Wed Jun 03 11:22:53 2015

3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 28 of 81	



1/4 Add connect to SOC
& EC

CPU THERMAL SENSOR



3/2 If HW shutdown,
QT1,RT1,R6011 need install,R9863 change to NI

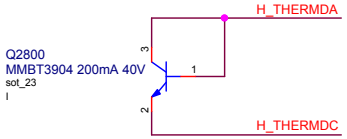


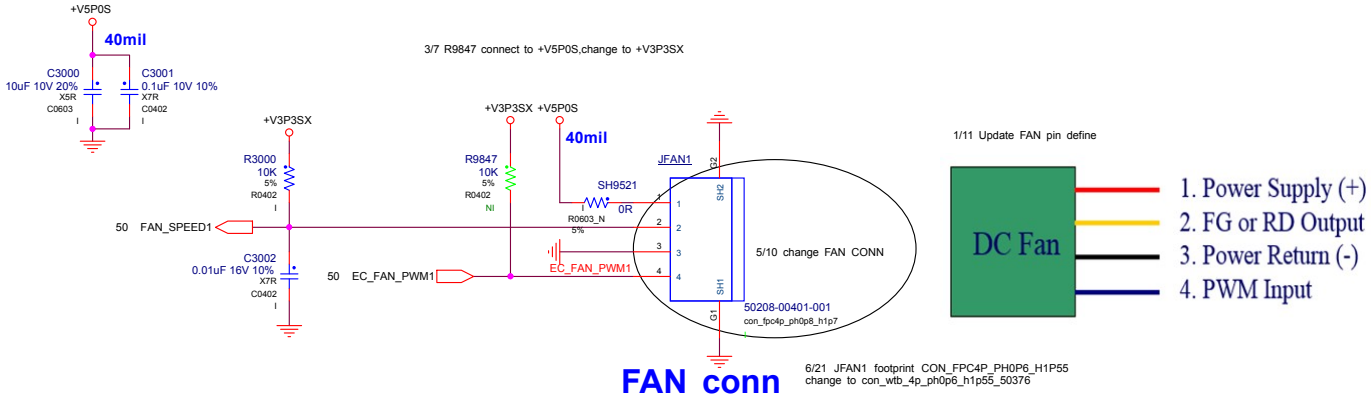
Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

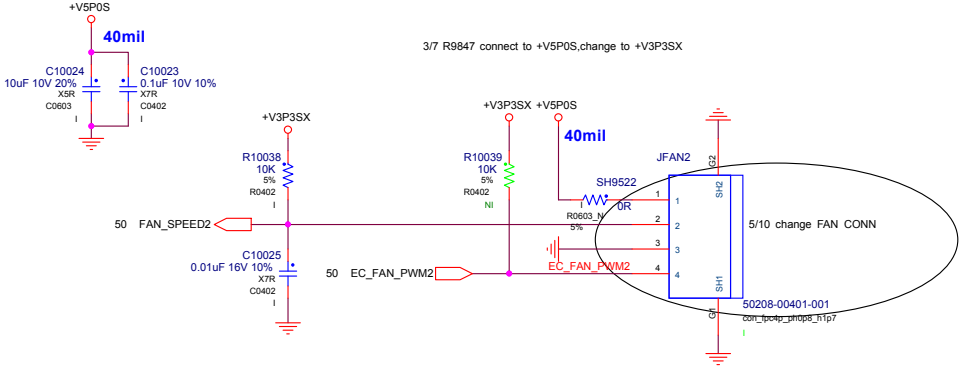
TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

+V3P3A +V3P3A 3,4,5,6,7,8,9,10,11,24,35,37,42,50,55,56,60,62,65,66,70

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size B	Title: CPU THERMAL SENSOR	Rev V01
Date: Monday, May 22, 2017	Sheet 29 of 81	



CIS ok



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: FAN conn	Rev: V01
Date: Wednesday, May 10, 2017	Sheet 30 of 81	

Project:	3205-13	
Engineer:	Jason	
Title:	3A	Rev.
		Lab
Date:	10/20/2014 2:01 PM	Sheet 31 of 31

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.32
Wed Jun 03 11:22:55 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 32 of 81	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd:+V1P0.33
Wed Jun 03 11:22:55 2015

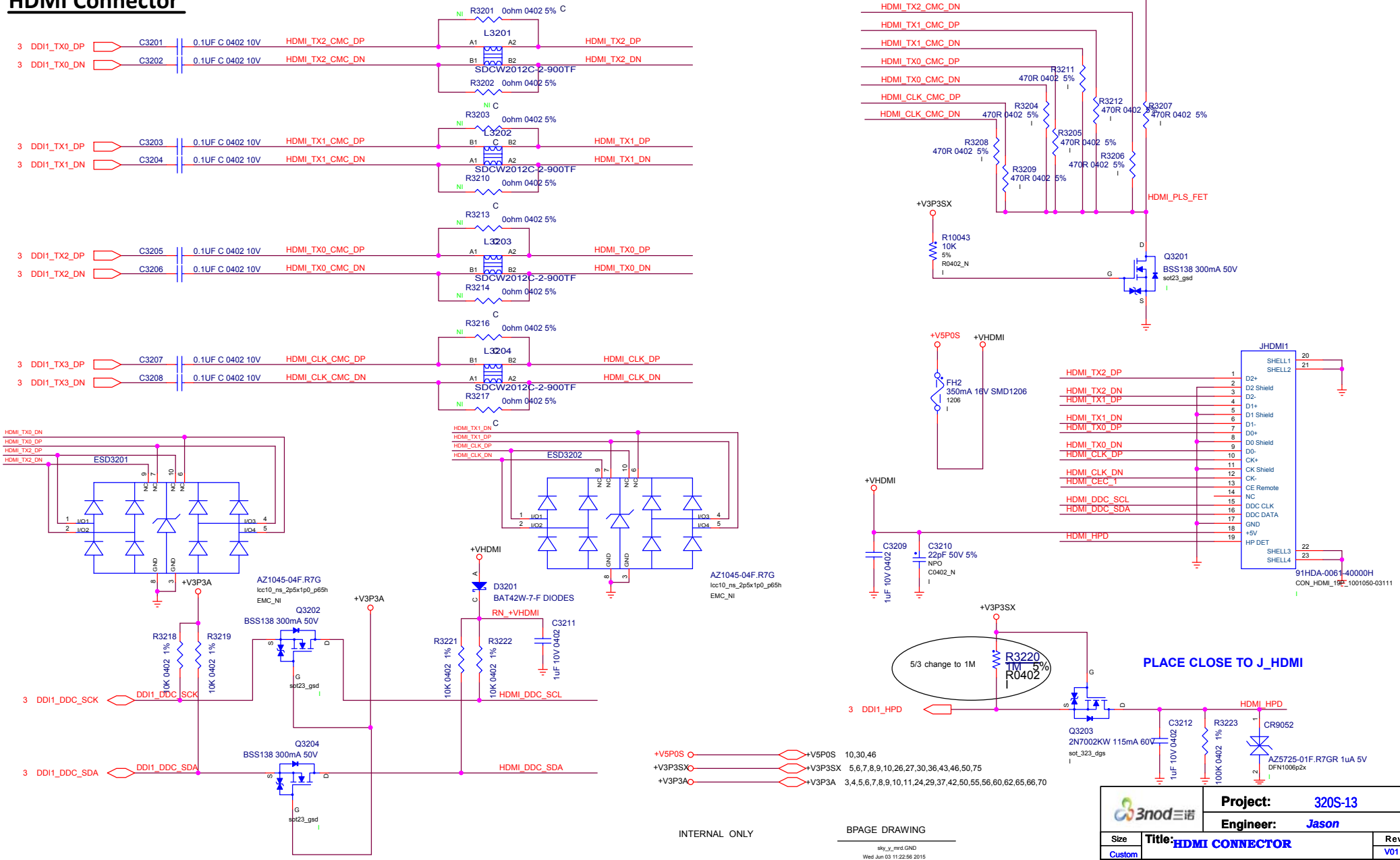
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 33 of 81	

Wed Jun 03 11:22:56 2015

3nod三诺	Project: 320S-13	
	Engineer: *Jason*	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 34 of 81	

HDMI Connector

for EMI Co-lay



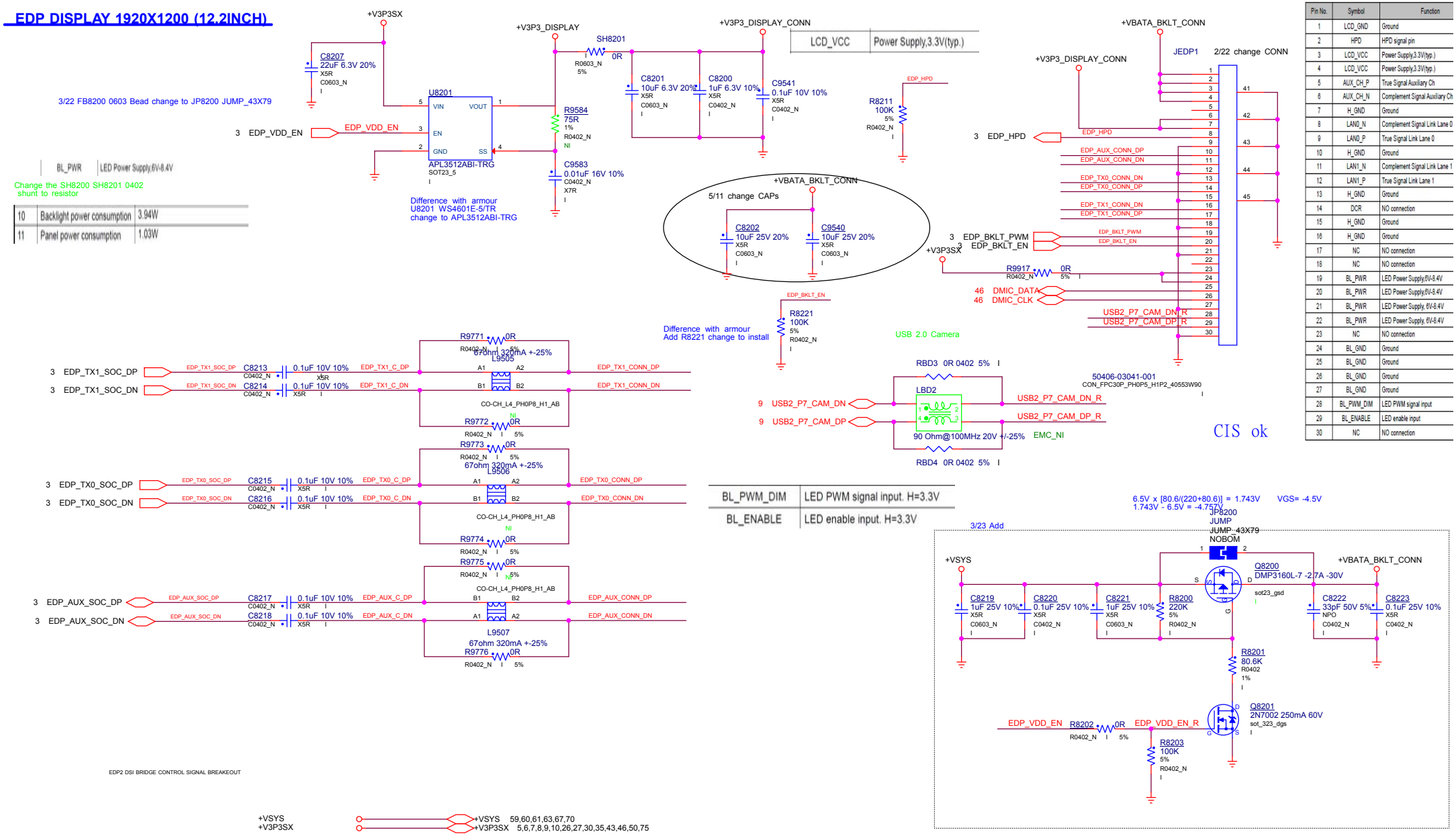
INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.GND
Wed Jun 03 11:22:56 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: HDMI CONNECTOR	Rev: V01
Date: Monday, May 22, 2017	Sheet 35 of 81	

EDP DISPLAY 1920X1200 (12.2INCH)

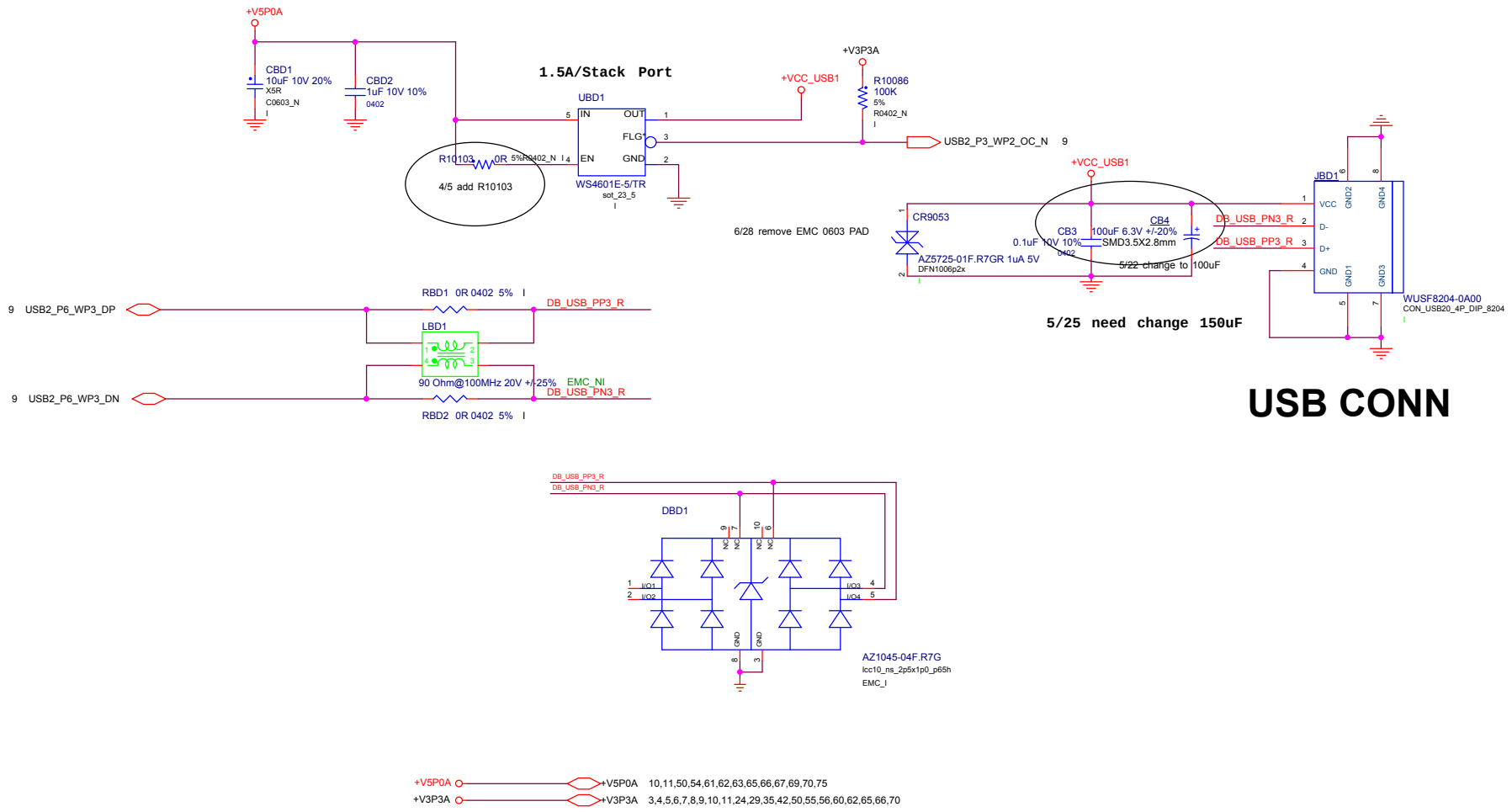


Intertace Pin Connection

Pin No.	Symbol	Function
1	LCD_GND	Ground
2	HPD	HPD signal pin
3	LCD_VCC	Power Supply,3.3V(typ.)
4	LCD_VCC	Power Supply,3.3V(typ.)
5	AUX_CH_P	True Signal Auxiliary Ch
6	AUX_CH_N	Complement Signal Auxiliary Ch
7	H_GND	Ground
8	LAN0_N	Complement Signal Link Lane 0
9	LAN0_P	True Signal Link Lane 0
10	H_GND	Ground
11	LAN1_N	Complement Signal Link Lane 1
12	LAN1_P	True Signal Link Lane 1
13	H_GND	Ground
14	DCR	NO connection
15	H_GND	Ground
16	H_GND	Ground
17	NC	NO connection
18	NC	NO connection
19	BL_PWR	LED Power Supply,6V-8.4V
20	BL_PWR	LED Power Supply,6V-8.4V
21	BL_PWR	LED Power Supply, 6V-8.4V
22	BL_PWR	LED Power Supply, 6V-8.4V
23	NC	NO connection
24	BL_GND	Ground
25	BL_GND	Ground
26	BL_GND	Ground
27	BL_GND	Ground
28	BL_PWM_DIM	LED PWM signal input
29	BL_ENABLE	LED enable input
30	NC	NO connection

3nod三诺	Project:	320S-13
	Engineer:	Jason
Size: Custom	Title: DISPLAY	Rev: V01
Date: Monday, May 15, 2017	Sheet 36 of 81	

USB2.0



USB CONN

BPAGE DRAWING

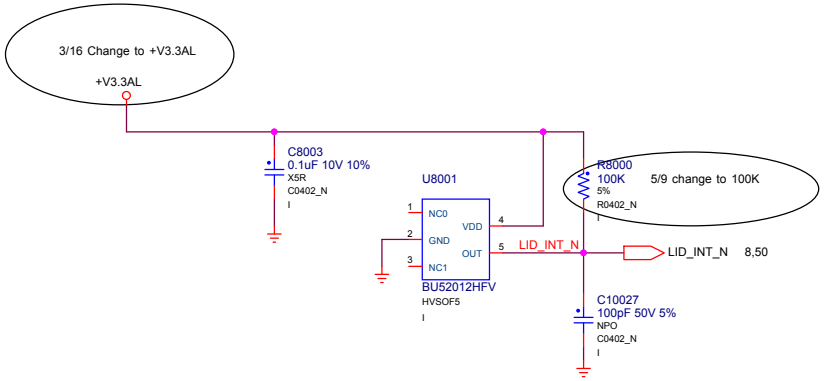
apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: USB2.0	Rev: V01
Date: Wednesday, June 28, 2017	Sheet 37 of 81	

Sensors

LID Sensor

Working voltage 2.4/ 2.7/ 5.5
max current 2.5mA typ:3uA



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: LID	Rev: V01
Date: Tuesday, June 20, 2017	Sheet 38 of 81	

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 39 of 81	

Wed Jun 03 11:22:59 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 40 of 81	

INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.41
Wed Jun 03 11:22:59 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 41 of 81	

USB3.0

+V5P0A 10,11,37,50,54,61,62,63,65,66,67,69,70,75
+V3P3A 3,4,5,6,7,8,9,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70

+V5CP — R10060 R0805_N 0R 5% I — +V5CP_R

3/29 Del CAP

4/20 change rating

CC452 22uF 6.3V 20% X5R C0603_N I

C3900 0.1uF 10V 10% X7R C0402_N I

5/23 change to 110K.

R3903 110K 1% R0402 I

R3902 20K 5% R0402_N I

+V3P3A — R3904 100K 5% R0402_N I — USB2_P1_WP0_OC_N 9

U3900 TPS2546RTER I

PwPd, ILIM_HI, ILIM_LO, GND, FAULT

IN, DM_OUT, DP_OUT, ILIM_SEL, OUT, DM_IN, DP_IN, STATE#, EN, CTL1, CTL2, CTL3

+V5P0A_USB_WP2

9 USB2_P1_WP1_DN
9 USB2_P1_WP1_DP

USB2_P1_DN
USB2_P1_DP

+V3.3AL 4/7 change from +V3P3A to +V3.3AL

R3958 100K 5% R0402_N I

USB_STATUS# — USB_STATUS# 50

TPS2546_CTL3 50
TPS2546_CTL2 50
TPS2546_CTL1 50

D+/D- ESD

USB2_P1_WP1_DP_CONN
USB2_P1_WP1_DN_CONN

CR9012 — AZ5725-01F.R7GR 1uA 5V DFN1006p2x EMC_I

CR9013 — AZ5725-01F.R7GR 1uA 5V DFN1006p2x EMC_I

+V3.3AL — R3900 100K 5% R0402 I

50 EC_ACDET — R3961 R0402_N 0R 5% I

R3901 0R R0402_N 5% NI

EC_USB_PWR_EN_R

R3960 0R R0402_N 5% I

50 EC_USB_PWR_EN

+V5P0A_USB_WP2

5/22 change to 100uF

C10022 100uF 6.3V +/-20% SMD3.5X2.8mm

C9006 470pF 50V 5% COG C0402_N I

C9007 4.7uF 10V 10% X5R C0603_N I

CR9054 — AZ5725-01F.R7GR 1uA 5V DFN1006p2x I

5/22 add ESD

CR9081 0R 5% NI R0603_N

JUSB3-1 — W-90-USB3-H082 con_usb3_9p_DIP_H6p9 I

VBUS, D-, D+, GND, STDA_SSRX-, STDA_SSRX+, GND_DRAIN, STDA_SSTX-, STDA_SSTX+, GND1, GND2, GND3, GND4

USB3_P1_TX_DP_CONN
USB3_P1_TX_DN_CONN
USB3_P1_RX_DN_CONN
USB3_P1_RX_DP_CONN

CR9006 — AZ1045-04F.R7G lcc10_ns_2p5x1p0_p65h EMC_I

R9007 0R R0402_N I 5%

L9003 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB NI

R9006 0R R0402_N I 5%

R9853 0R R0402_N I 5%

L9508 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB NI

R9852 0R R0402_N I 5%

9 USB3_P1_RX_DN
9 USB3_P1_RX_DP

R9012 0R R0402_N I 5%

L9002 67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB NI

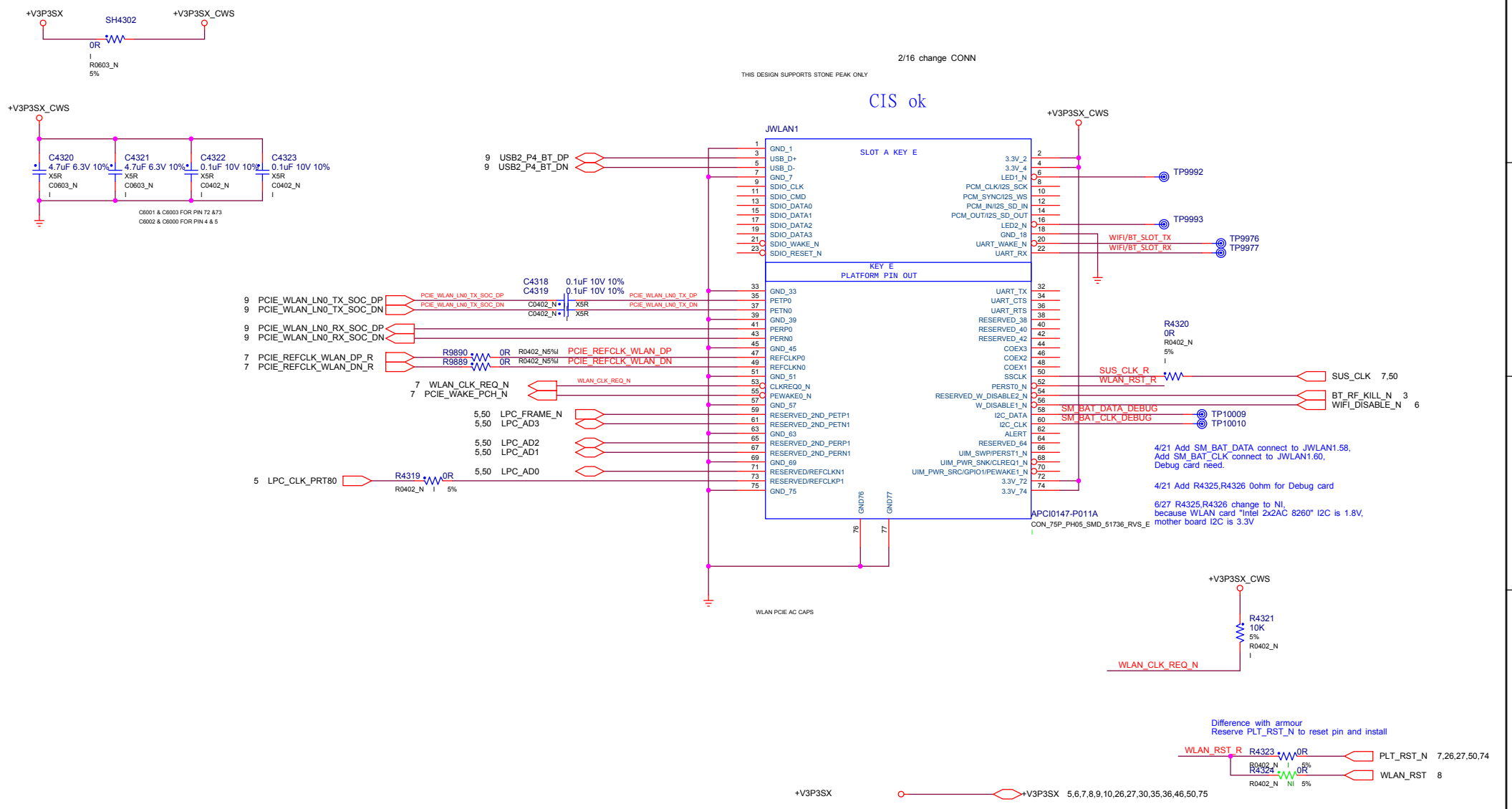
R9011 0R R0402_N I 5%

9 USB3_P1_TX_DN — C1271 C0402_N 0.1uF 10V 10% X5R USB3_P1_TX_DN_C
9 USB3_P1_TX_DP — C1270 C0402_N 0.1uF 10V 10% X5R USB3_P1_TX_DP_C

+V3.3AL — +V3.3AL 11,38,46,50,51,58,60
+V5CP — +V5CP 10,60
+V3P3A — +V3P3A 3,4,5,6,7,8,9,10,11,24,29,35,37,42,50,55,56,60,62,65,66,70

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: USB3.0 CONN	Rev: V01
Date: Tuesday, May 23, 2017	Sheet 42 of 81	

WIFI & BT Module



INTERNAL ONLY

BPAGE DRAWING

sky_y_mrd.+V3P3.43
Wed Jun 03 11:23:00 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: WLAN WIFI BT MODULE	Rev: V01
Date: Monday, April 10, 2017	Sheet 43 of 81	

Project:	320S-13
Engineer:	Jason
Size: Custom	Title: NA
Rev	V01
Date:	Monday, April 10, 2017
Sheet	44 of 81

INTERNAL ONLY

BPAGE DRAWING

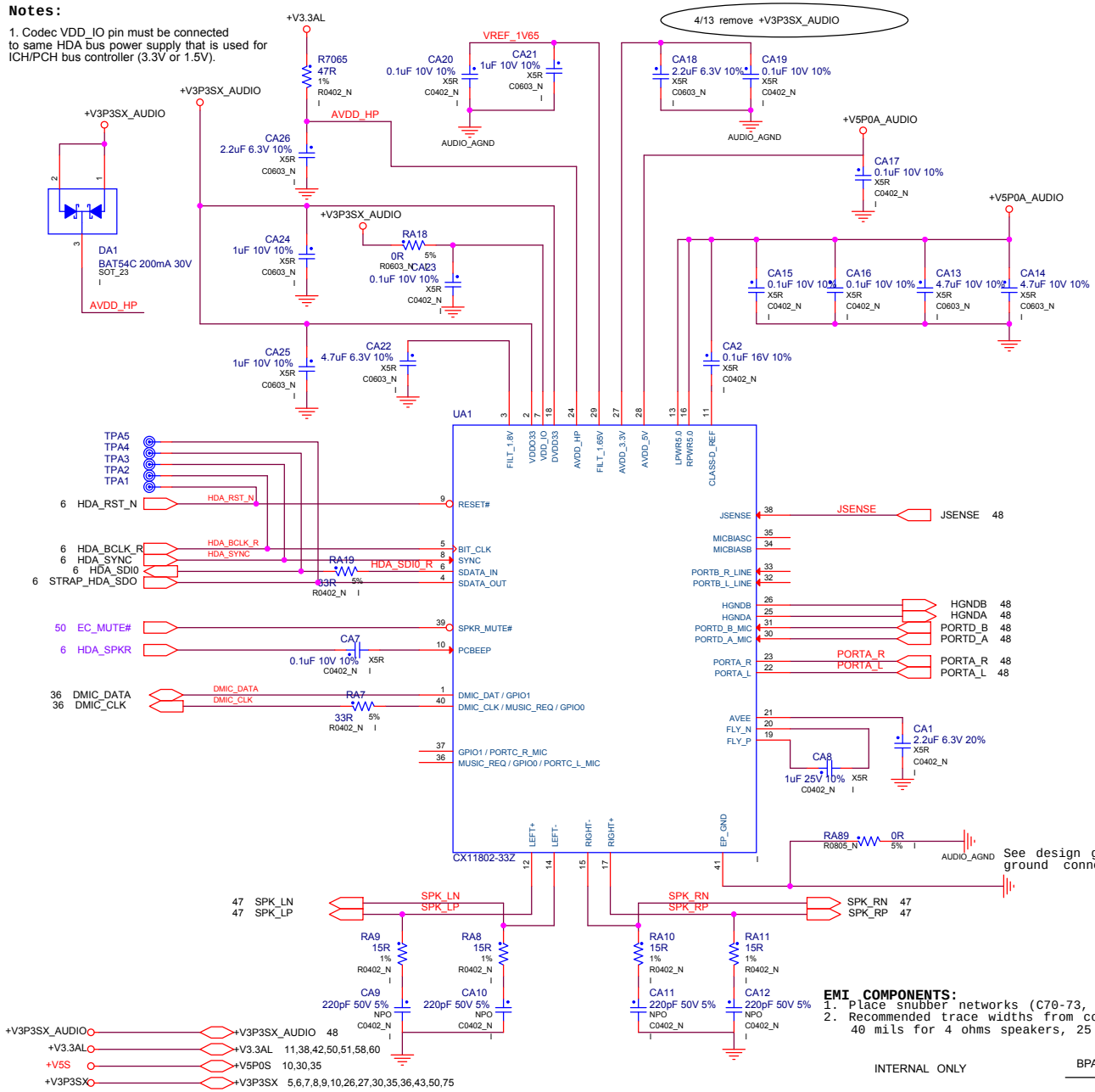
sky_v_mrd.GND
Wed Jun 03 11:23:01 2015

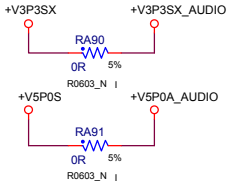
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 45 of 81	

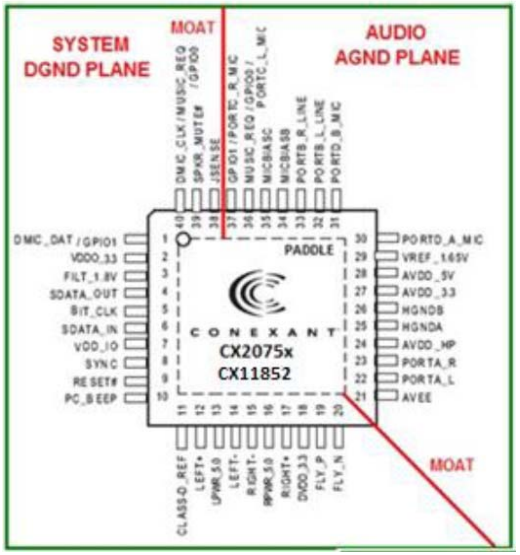
Notes:

1. Codec VDD_IO pin must be connected to same HDA bus power supply that is used for ICH/PCH bus controller (3.3V or 1.5V).

4/13 remove +V3P3SX_AUDIO







EMI COMPONENTS:
1. Place snubber networks (C70-73, R70-73) very close to codec pins.
2. Recommended trace widths from codec to speakers are 40 mils for 4 ohms speakers, 25 mils for 8 ohms.

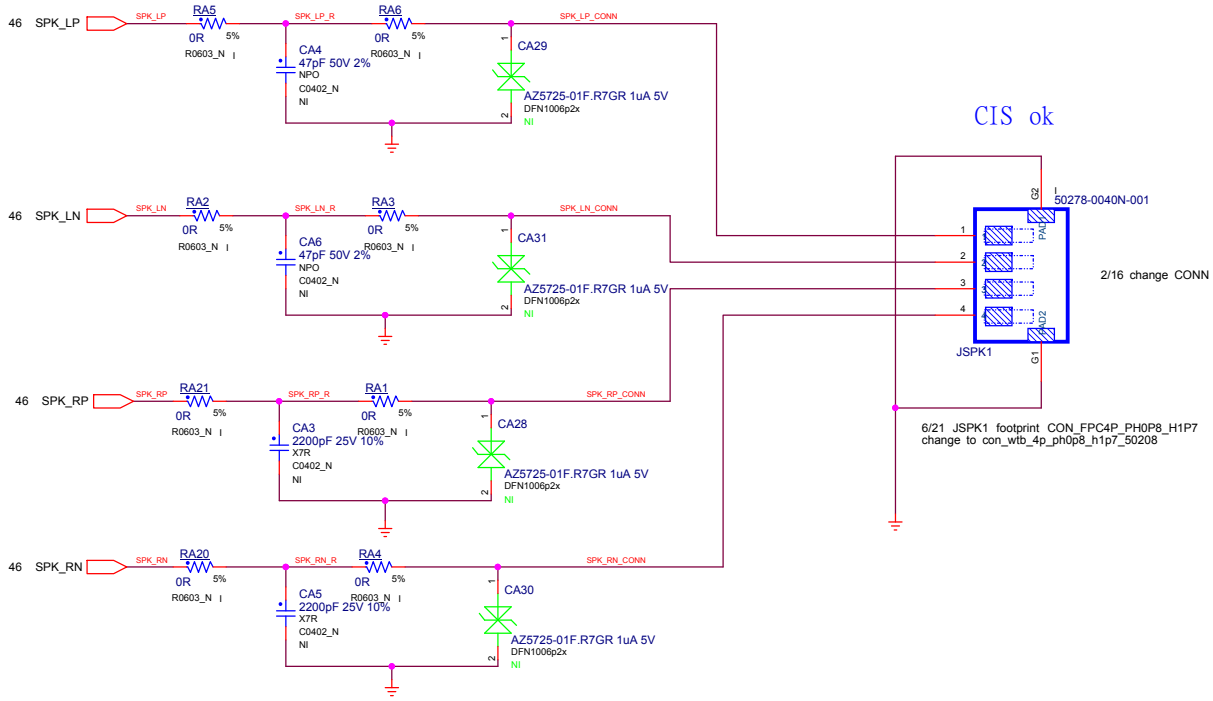
INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:22 2016

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: <AUDIO CODEC>	Rev: V01
Date: Thursday, April 13, 2017	Sheet 46 of 81	

Speaker



CIS ok

2/16 change CONN

6/21 JSPK1 footprint CON_FPC4P_PH0P8_H1P7
change to con_wtb_4p_ph0p8_h1p7_50208

INTERNAL ONLY

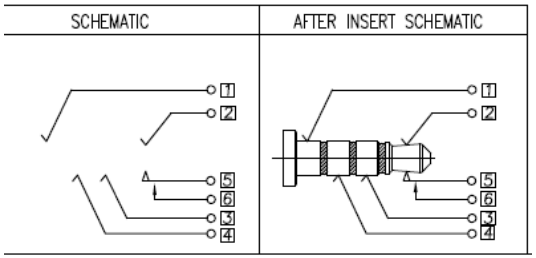
BPAGE DRAWING

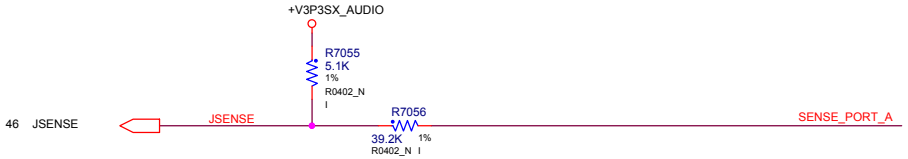
sky_v_mrd.GND
Wed Jun 03 11:23:02 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: Speaker	Rev: V01
Date: Monday, April 10, 2017	Sheet 47 of 81	

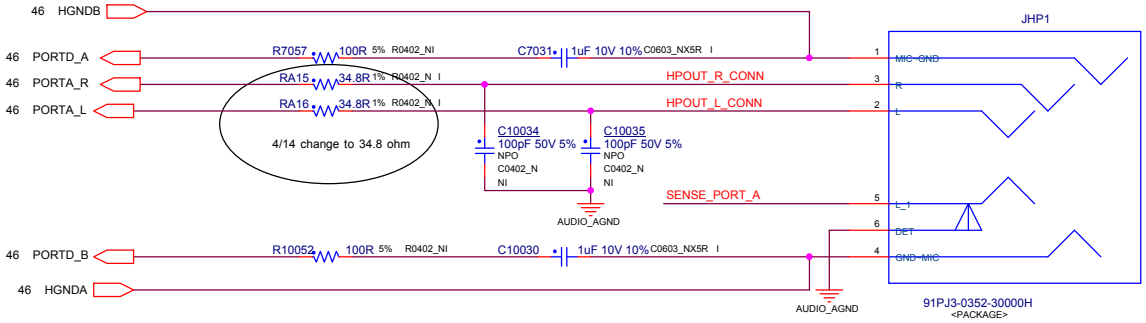
HEADSET JACK (Supports CTIA and OMTP headsets)

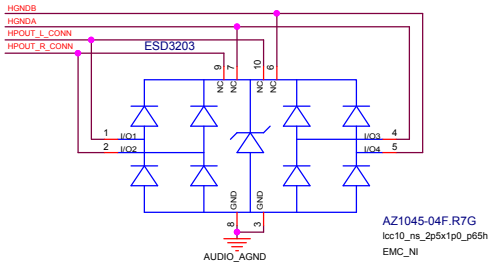
Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.

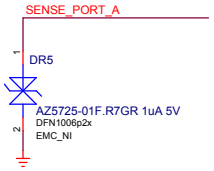




2/22 change CONN







INTERNAL ONLY

BPAGE DRAWING

apl_lE.8A
Fri May 27 06:47:24 2016

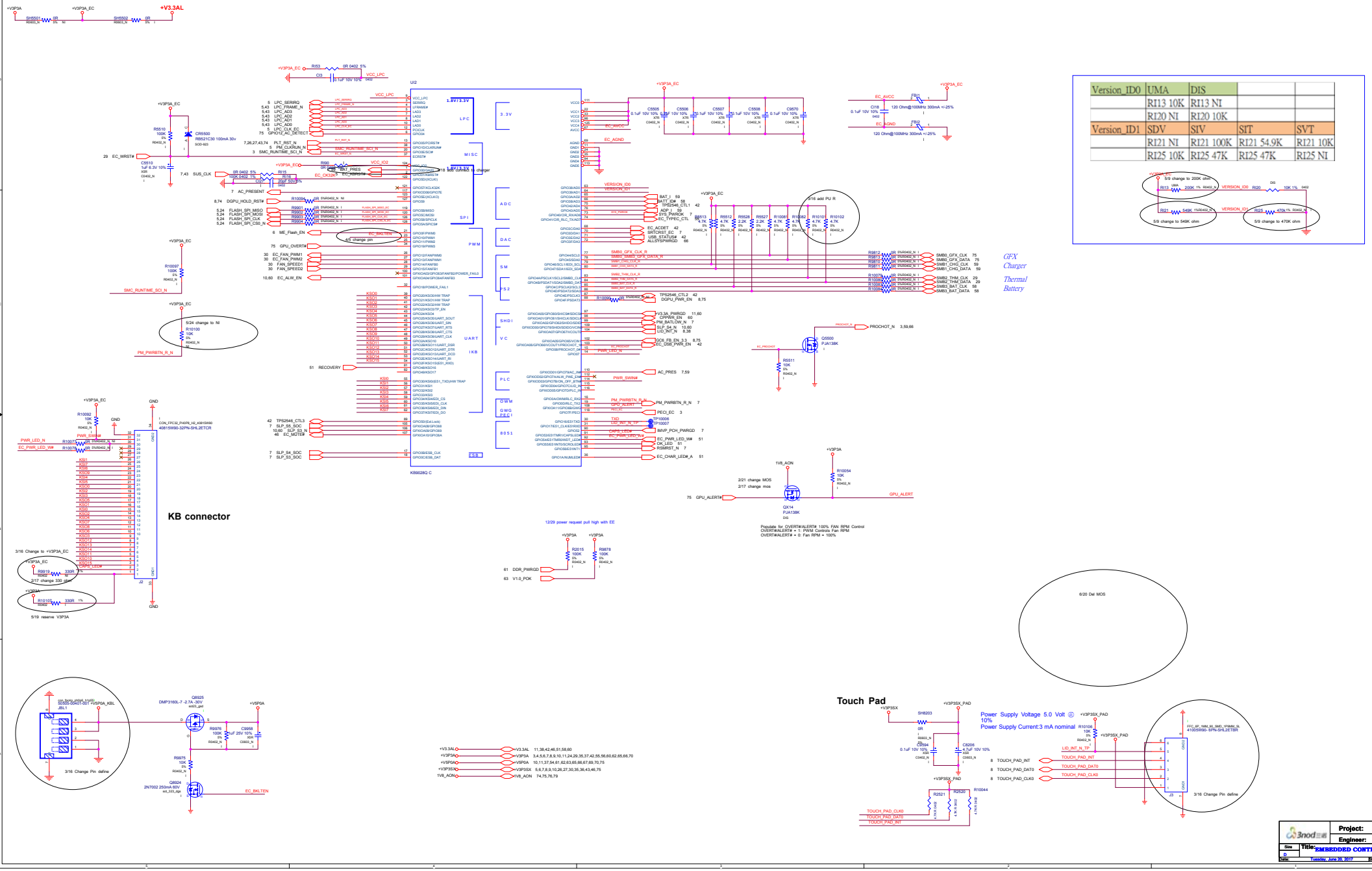
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: <AUDIO_HEADSET>	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 48 of 81	

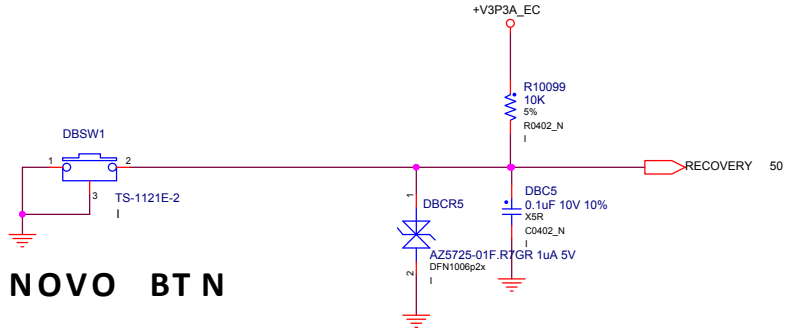
BPAGE DRAWING

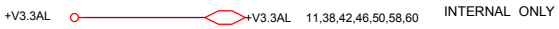
sky_y_mrd.+VCHG.49
Wed Jun 03 11:23:03 2015

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 49 of 81	

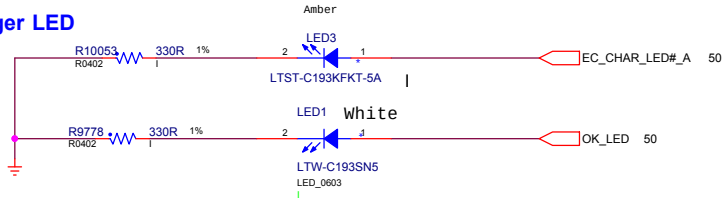
EC controller



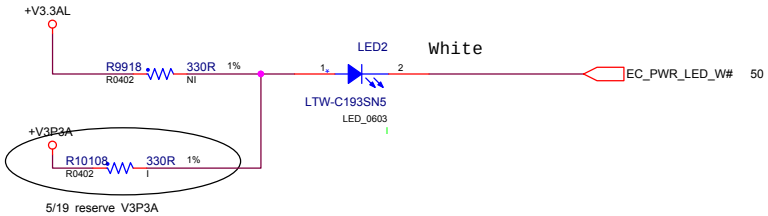




Charger LED



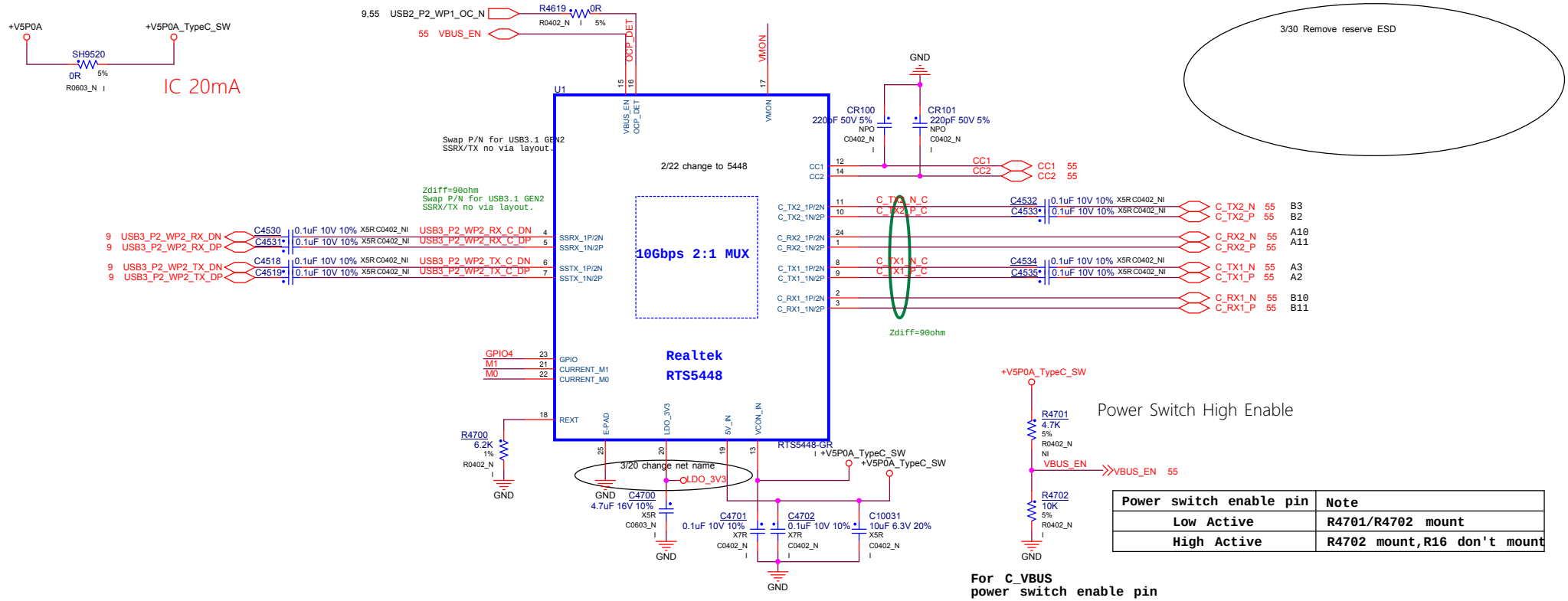
SYS LED



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: BUTTON & LED	Rev: V01
Date: Tuesday, May 23, 2017	Sheet 51 of 81	

3nod三诺	Project: 320S-13
	Engineer: Jason
Size: Custom	Title: NA
	Rev: V01
Date: Monday, April 10, 2017	Sheet 52 of 81

3nod三诺	Project: 320S-13
	Engineer: Jason
Size: Custom	Title: NA
Rev	V01
Date: Monday, April 10, 2017	Sheet 53 of 81



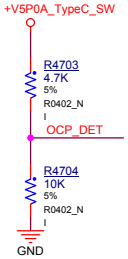
3/30 Remove reserve ESD

Power Switch High Enable

Power switch enable pin	Note
Low Active	R4701/R4702 mount
High Active	R4702 mount,R16 don't mount

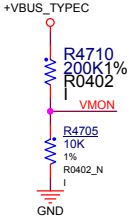
For C_VBUS
power switch enable pin

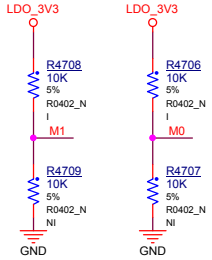
OCP Low Enable



Power switch OCP pin	Note
Low Active	R4704/R4703 mount
High Active	R4704 mount,R4703 don't mount

For C_VBUS
power switch OCP pin



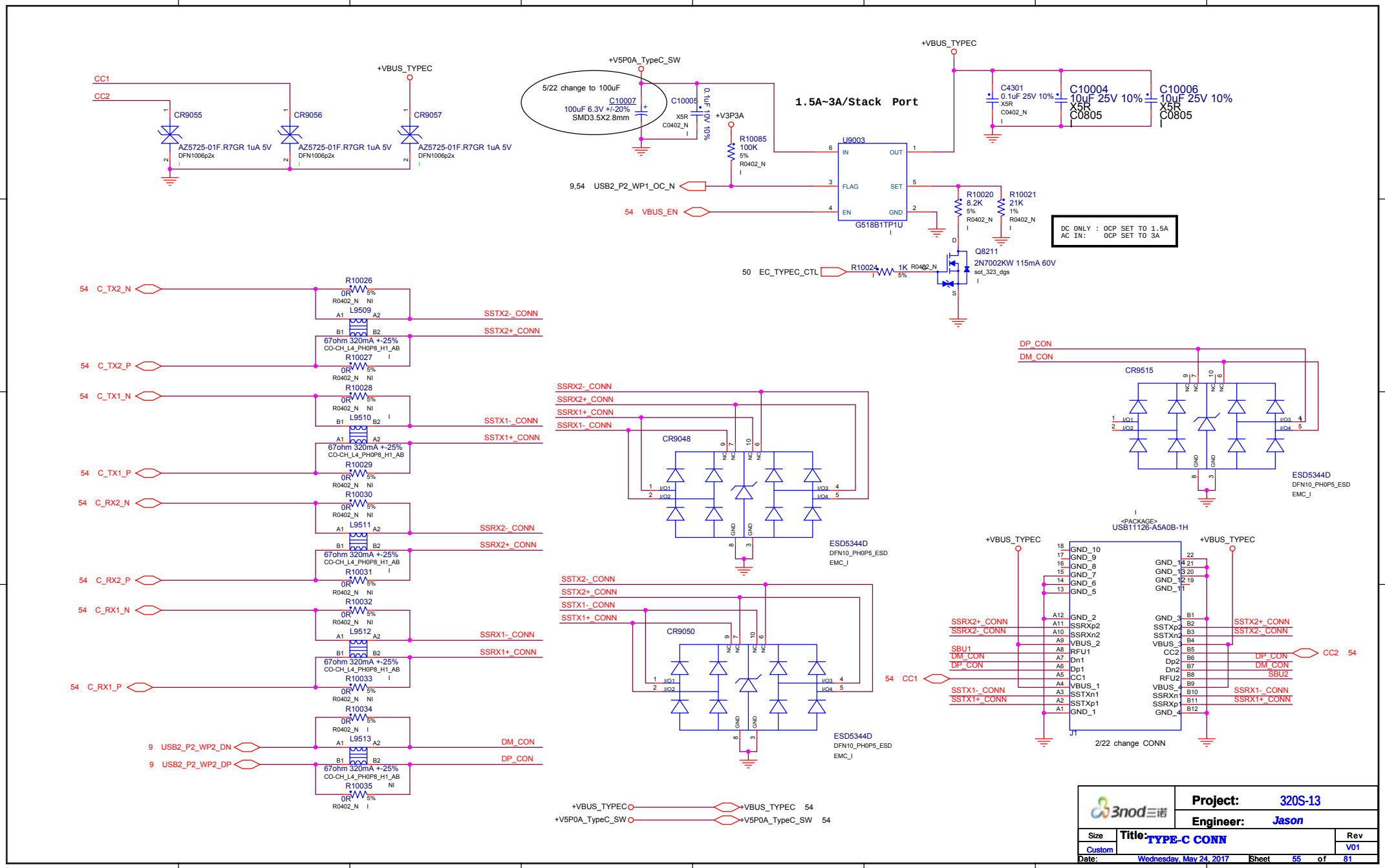


Rp configuration

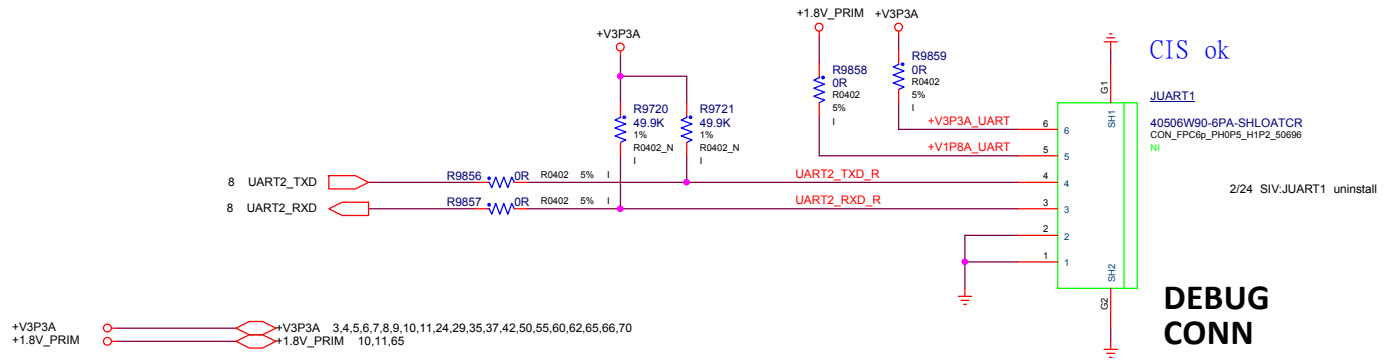
	M1	M0	Note
Rp:900mA	0	1	R11/R12 mount,R10/R13 don't mount
Rp:1.5A	1	0	R10/R13 mount,R11/R12 don't mount
Rp:3.0A	1	1	R10/R12 mount,R11/R13 don't mount

Rp:1.5A (now)

3nod三诺	Project: 320S-13		
	Engineer: Jason		
Size: Custom	Title: TYPE-C Switch		Rev: V01
Date: Monday, April 10, 2017	Sheet 54 of 81		

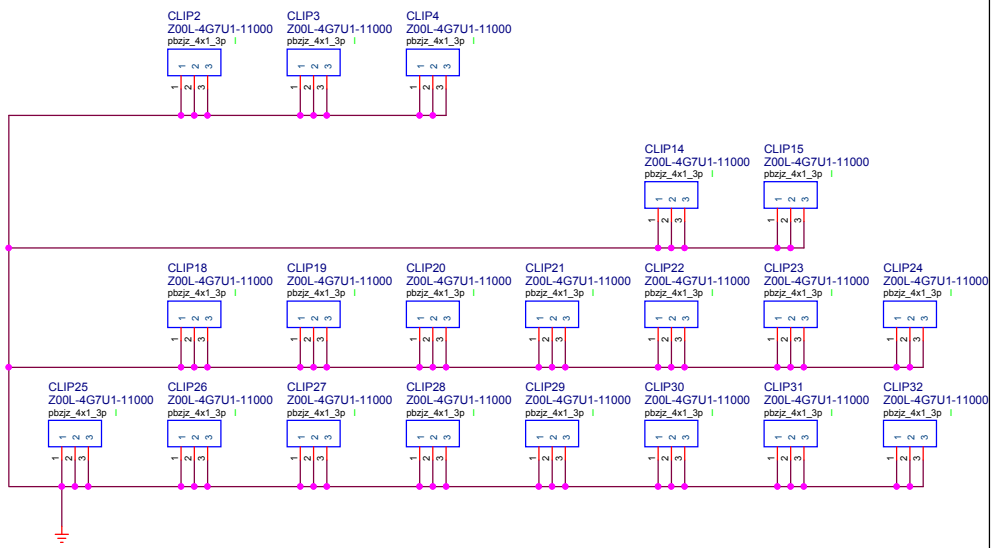


3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: TYPE-C CONN	Rev: V01
Date: Wednesday, May 24, 2017	Sheet 55 of 81	

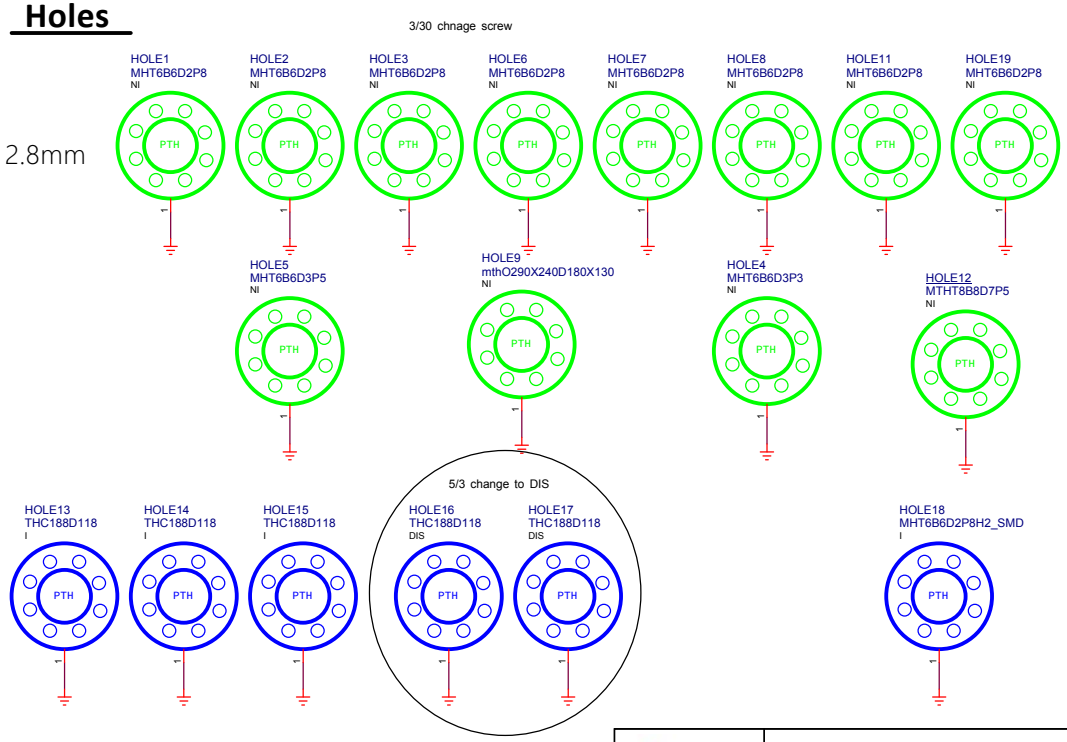


DEBUG CONN

Shielding



Holes



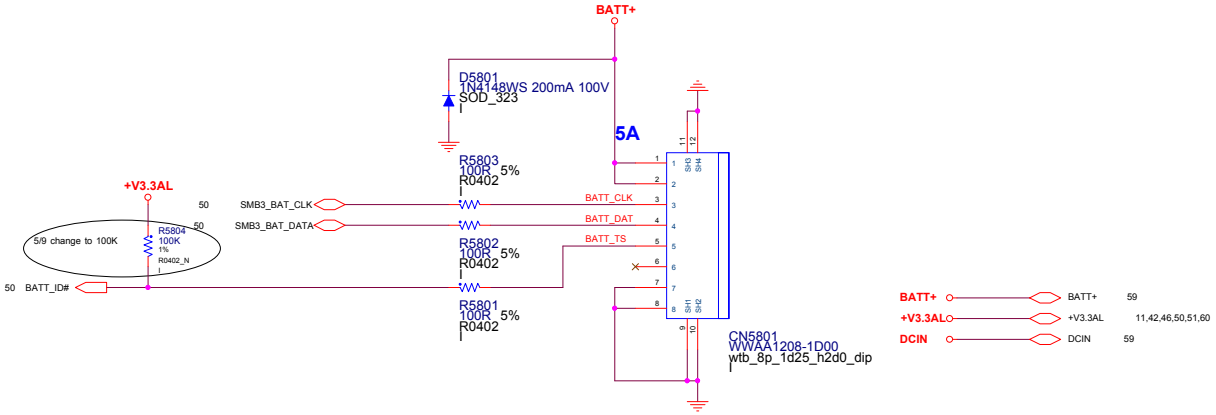
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: UART CONN & HOLE & CLIP	Rev: V01
Date: Friday, May 12, 2017	Sheet 56 of 81	

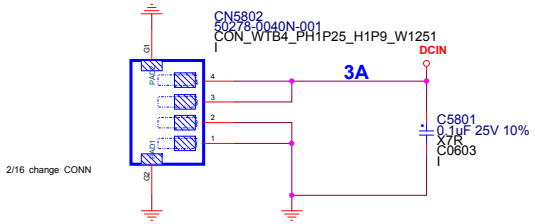
EVT=>SIV

No.	Change details	Change Reason
1	LID_INT_N change PU to +V3.3AL.	EC need recognize LID in S5.
2	Change KBL CONN Pin define.	EVT CE not confirm the Pin define correct.
3	Change Touch PAD Pin define.	Touch PAD SPEC update, add LID control Pin.
4	Change Keyboard power LED voltage to +V3.3AL.	Synchronize with System LED.
5	Type C IC Pin.20 change to LDO_3V3.	LDO_3V3 lose connection.
6	Install R574,R537.	Install for GPU.
7	remove DR3,DR4.	unnecessary
8	Change UBD2 solution.	for support 1V voltage
9	Add PU for SMB2_THM_CLK,DATA.	lose SMB PU
10	remove C10026.	unnecessary

3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size C	Title: HW Change list	Rev V01
Date: Monday, April 10, 2017	Sheet 57 of 81	

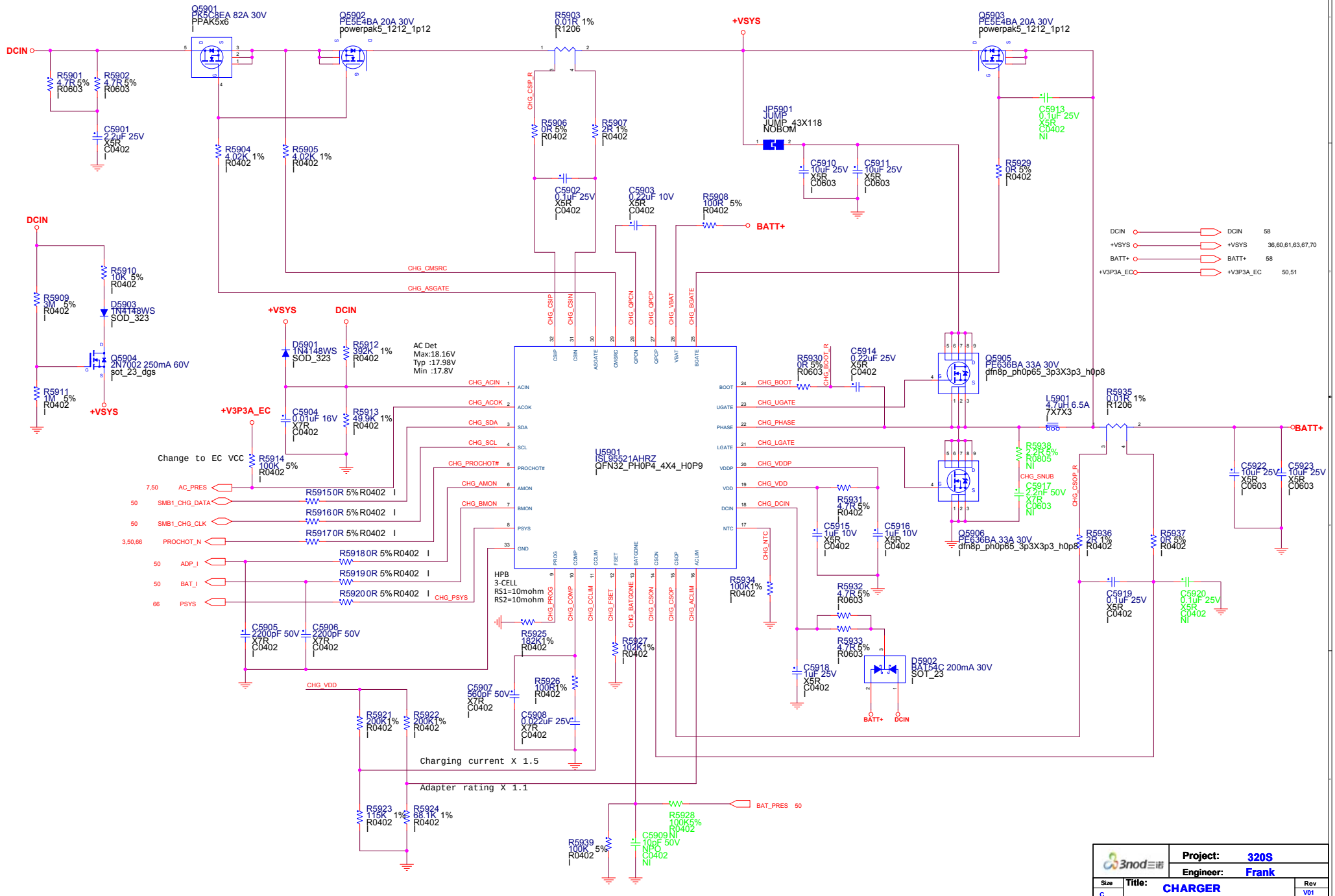
58: BATTERY CONNECTOR



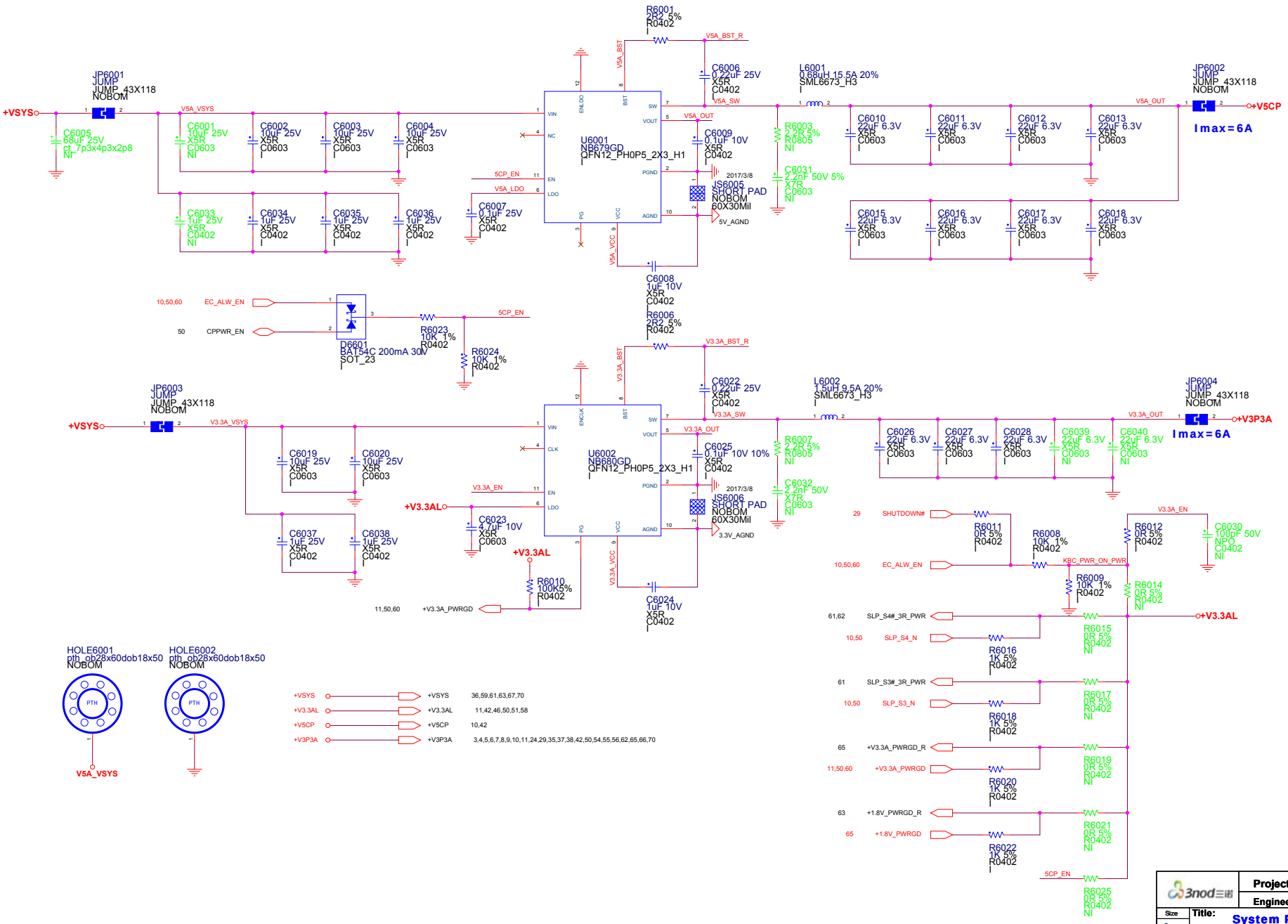


3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: BATT CONN	Rev V01
Date: Tuesday, June 20, 2017	Sheet 58 of 81	

59: BATTERY CHARGER

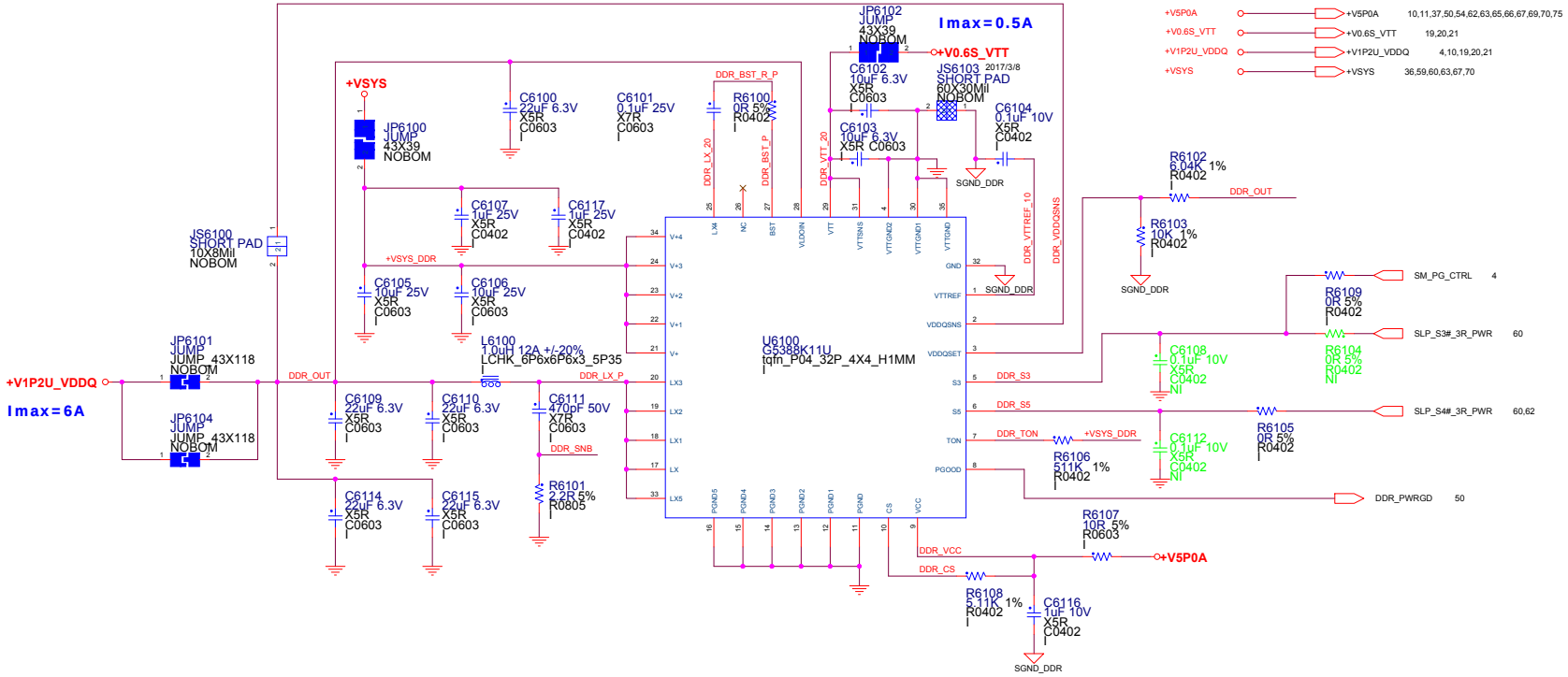


60: +V5P0A / +V3P3A POWER SUPPLY



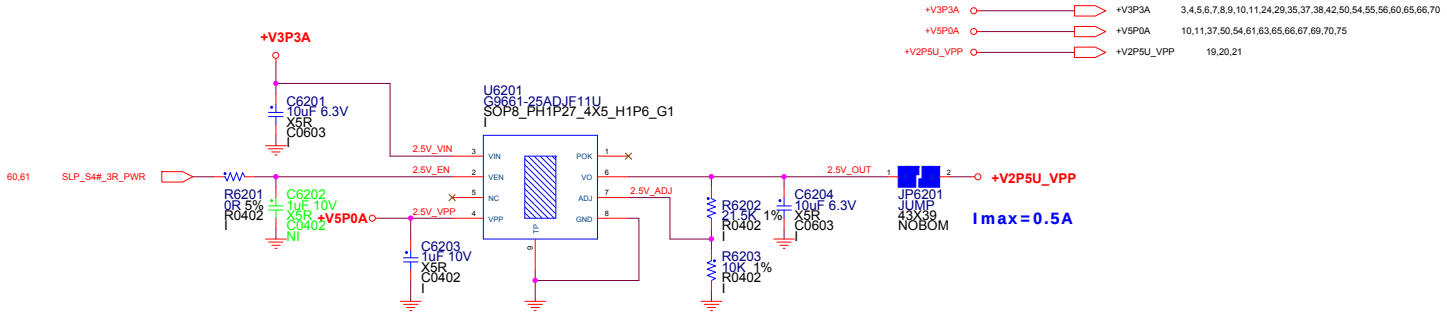
3nod三诺	Project: 320S		
	Engineer: Frank		
Size C	Title: System Power		Rev V01
Date: Tuesday, June 27, 2017	Sheet 60 of 81		

61: DDR POWER SUPPLY



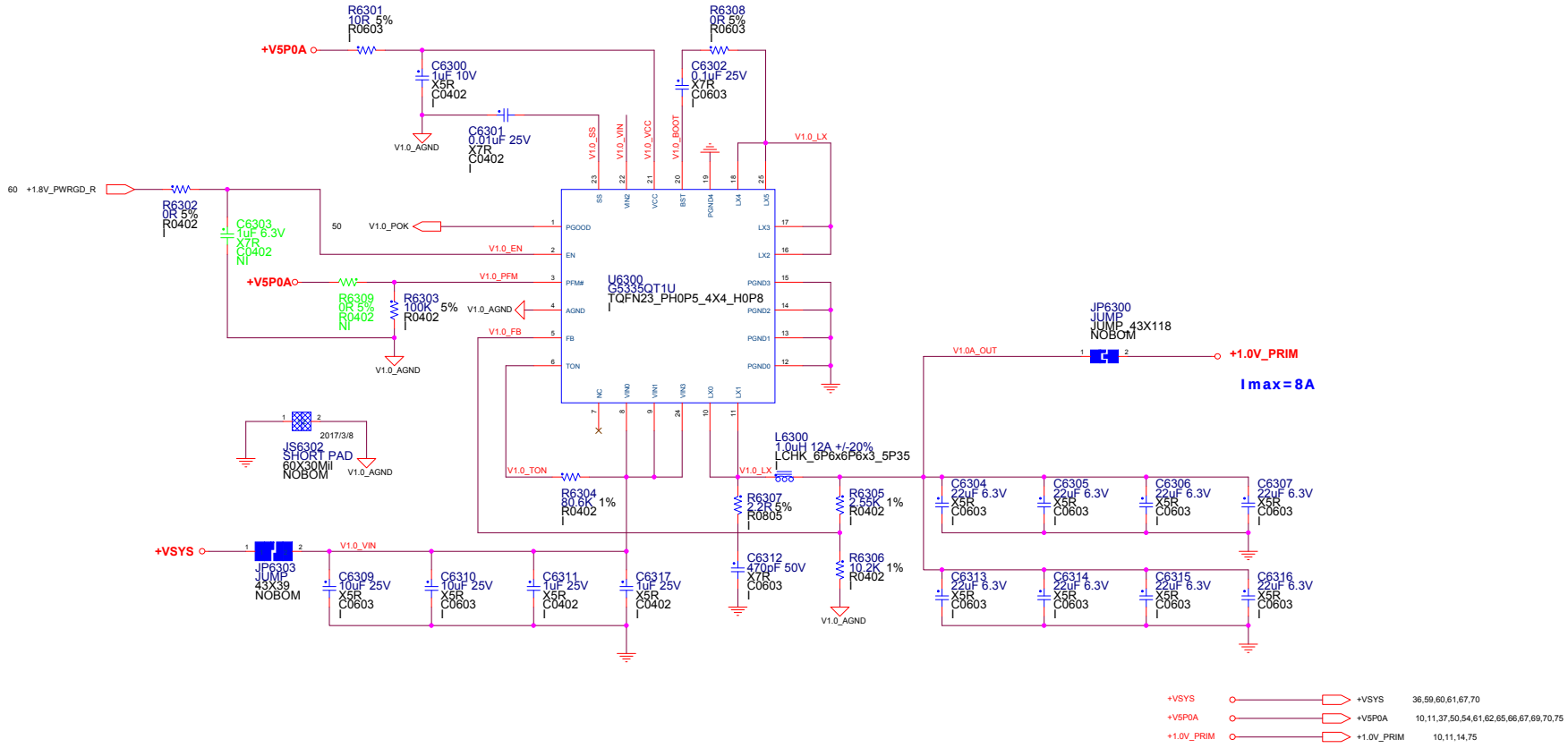
3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: DDR Power	Rev V01
Date: Wednesday, May 31, 2017	Sheet 61 of 81	

62: +V2P5U_VPP POWER SUPPLY



3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: +V2P5U_VPP	Rev V01
Date: Thursday, June 01, 2017	Sheet 62 of 81	

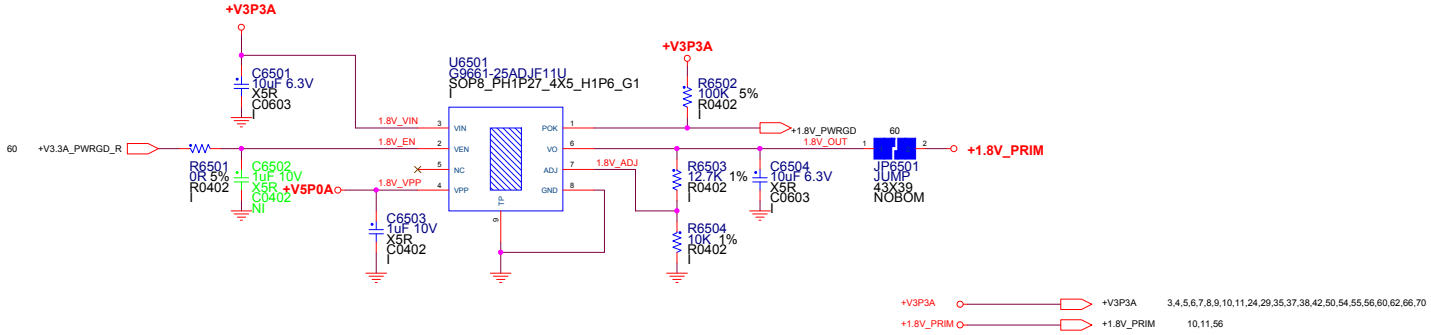
63: +1.0V_PRIM POWER SUPPLY



3nod三诺	Project: 320S	
	Engineer: Frank	
Size: C	Title: +1.0V_PRIM	Rev: V01
Date: Wednesday, May 31, 2017	Sheet 63 of 81	

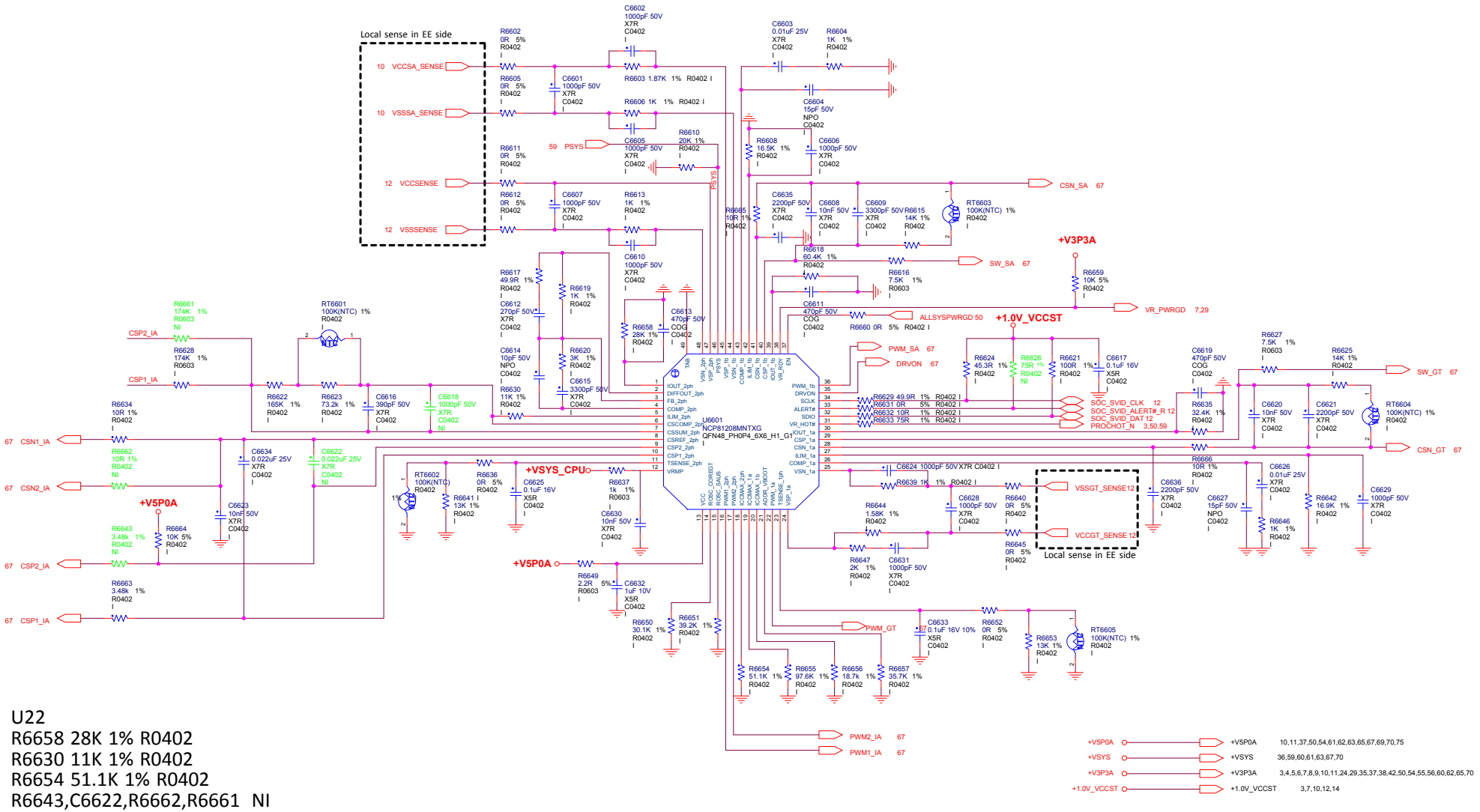
3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: NA	Rev V01
Date: Monday, May 15, 2017	Sheet 64 of 81	

65: +1.8V_PRIM POWER SUPPLY



3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: +1.8V_PRIM	Rev V01
Date: Thursday, June 01, 2017	Sheet 65 of 81	

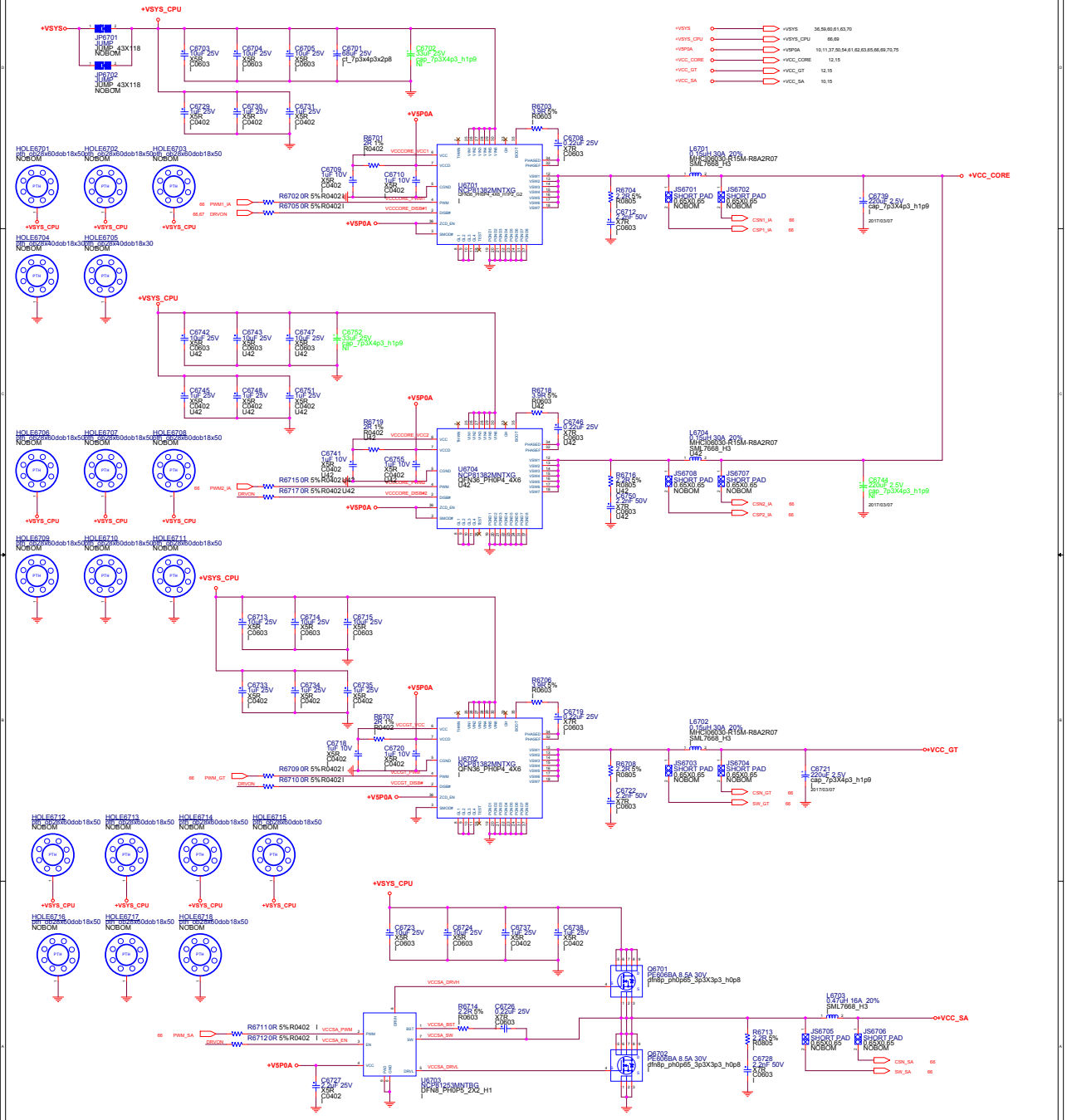
66: CPU POWER SUPPLY



U22
R6658 28K 1% R0402
R6630 11K 1% R0402
R6654 51.1K 1% R0402
R6643,C6622,R6662,R6661 NI
R6664 I

3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: CPU VR IC	Rev V01
Date: Thursday, June 22, 2017	Sheet 66 of 72	

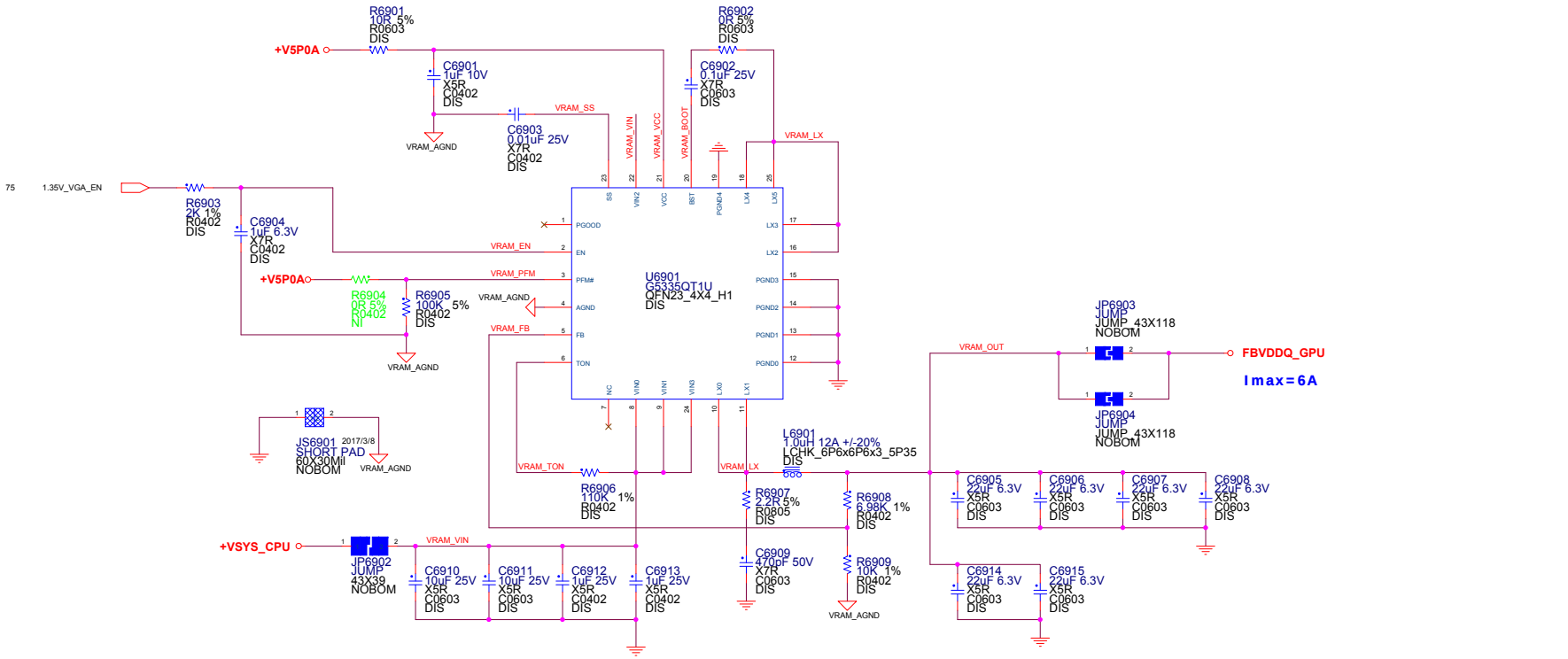
67: VCC_CORE / GT / SA POWER SUPPLY



Project: 320S		
Engineer: Frank		
Size: Custom	Title: VCC_CORE / GT / SA	Rev: V01
Date: Tuesday, June 27, 2017	Sheet 67 of 81	

3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: NA	Rev V01
Date: Monday, May 15, 2017	Sheet 68 of 81	

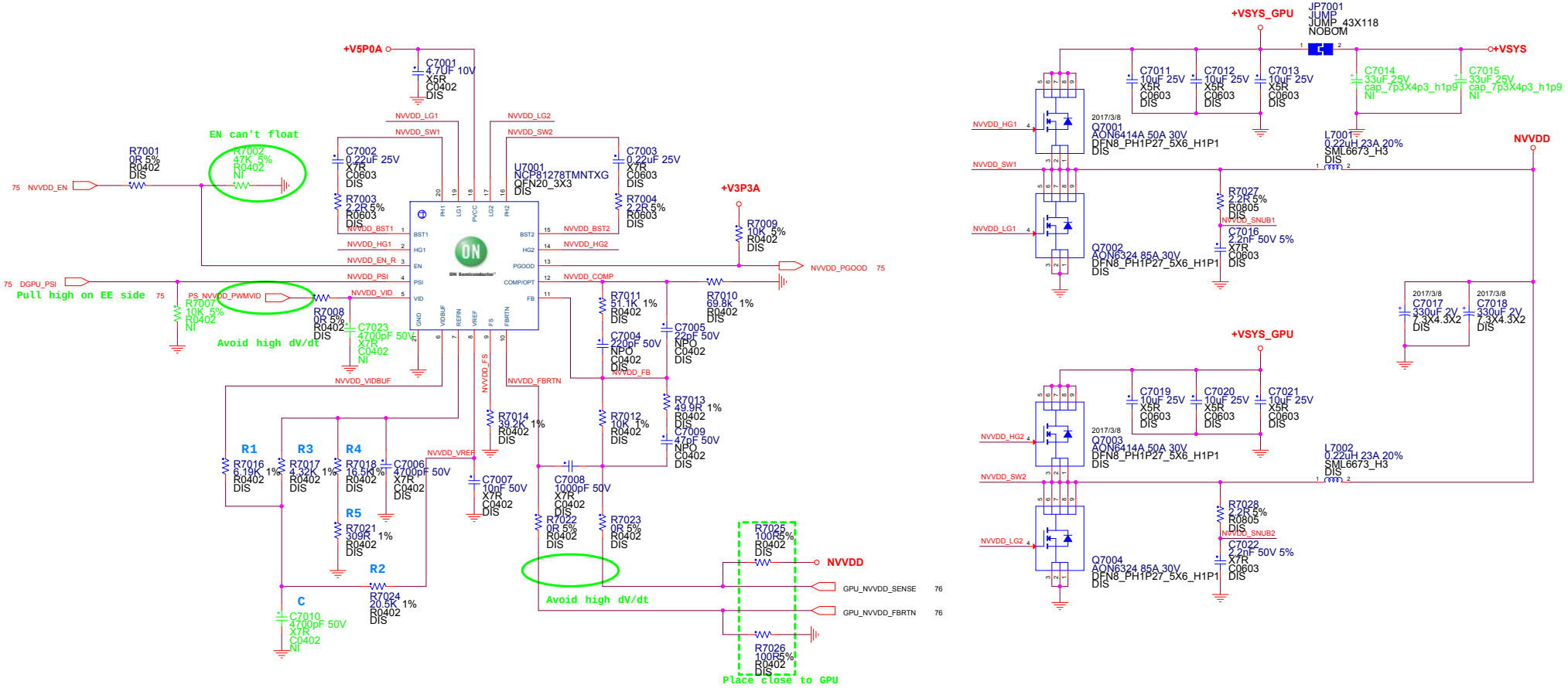
69: VRAM POWER SUPPLY



+VSYS_CPU	+VSYS_CPU	66,67
+V5P0A	+V5P0A	10,11,37,50,54,61,62,63,65,66,67,70,75
FBVDDQ_GPU	FBVDDQ_GPU	76,78,79,80

3nod三诺	Project: 320S	
	Engineer: Frank	
Size: C	Title: VRAM POWER SUPPLY	Rev: V01
Date: Wednesday, May 31, 2017	Sheet 69 of 81	

70: GPU POWER NVVDD



3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: GPU NVVDD	Rev V01
Date: Wednesday, May 31, 2017	Sheet 70 of 81	

3nod三诺	Project: 320S	
	Engineer: Frank	
Size C	Title: NA	Rev V01
Date: Monday, May 15, 2017	Sheet 71 of 81	

POWER CHANGE LIST
SDV to SIV

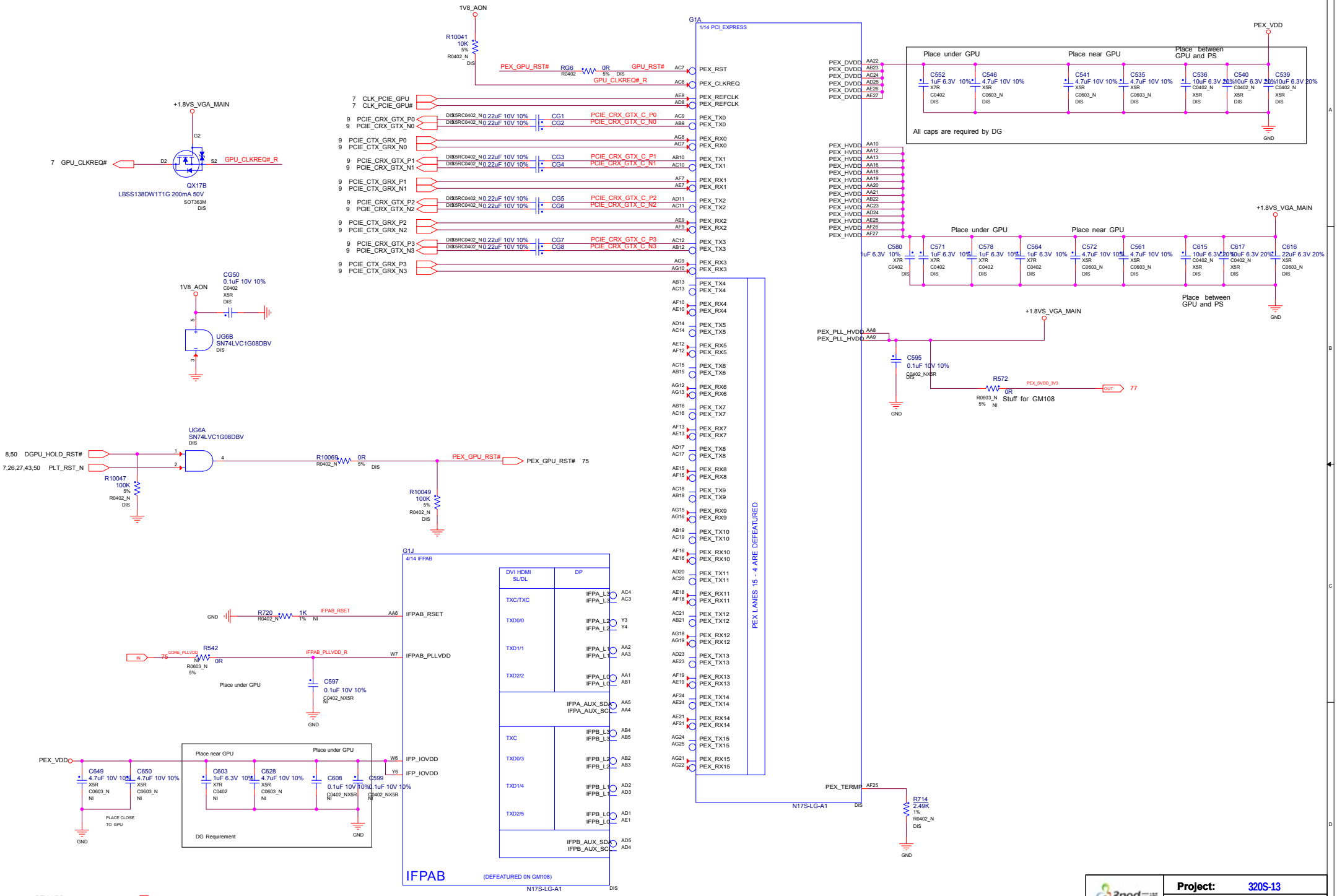
2017/4/6
Page 59.
Fine tune charger schematic to fix ACOK is abnormal issue.
Change L5901 from 3.3uH to 4.7uH.
R5936 from 1R0 to 2R0.
R5937 from 1R0 to 0ohm.
R5923 from 90.9K to 115K.
C5920 NI.

Page 66.
Fine tune CPU VR IC RC for transient.(U22)
R6658 change from 25.5K to 28K.
R6619 change from 604R to 1K.
R6630 change from 20K to 11K.
R6654 change from 100K to 51.1K.
R6656 change from 15.8K to 18.7K.
R6644 change from 1.65K to 1.58K.
R6646 changed from 1.5K to 1K.
R6635 changed from 30.9K to 32.4K.
C6621 changed from 680pF to 2200pF.
R6618 changed from 69.8K to 60.4K.
R6661,R6662,R6643,C6622 NI
R6664 I

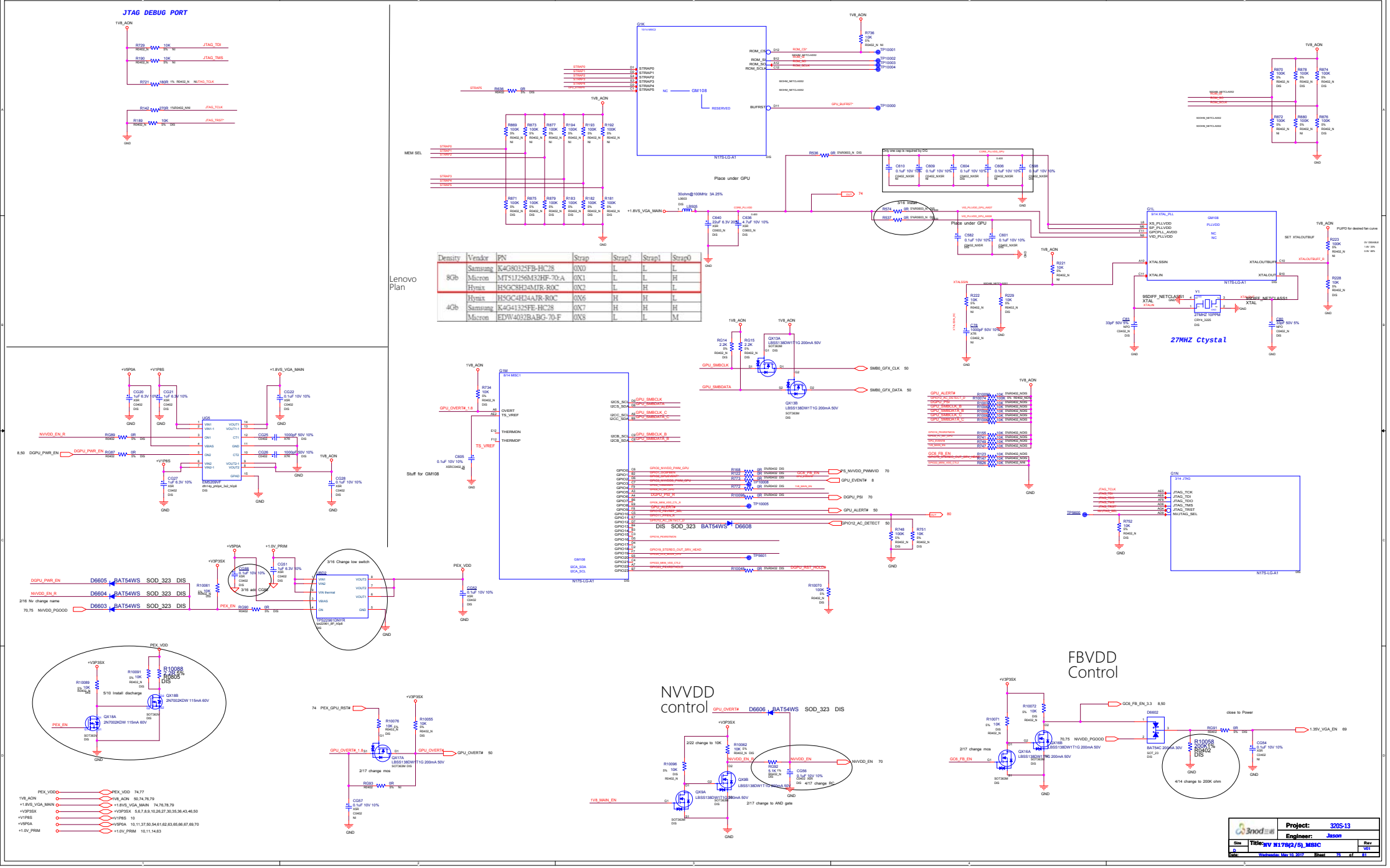
Page 70.
Fine tune OCP.
R7010 change from 51.1K to 69.8K.

3nod三诺	Project: 320S	
	Engineer: Frank	
Size: C	Title: PWR Change List	Rev: V01
Date: Monday, May 15, 2017	Sheet 72 of 81	

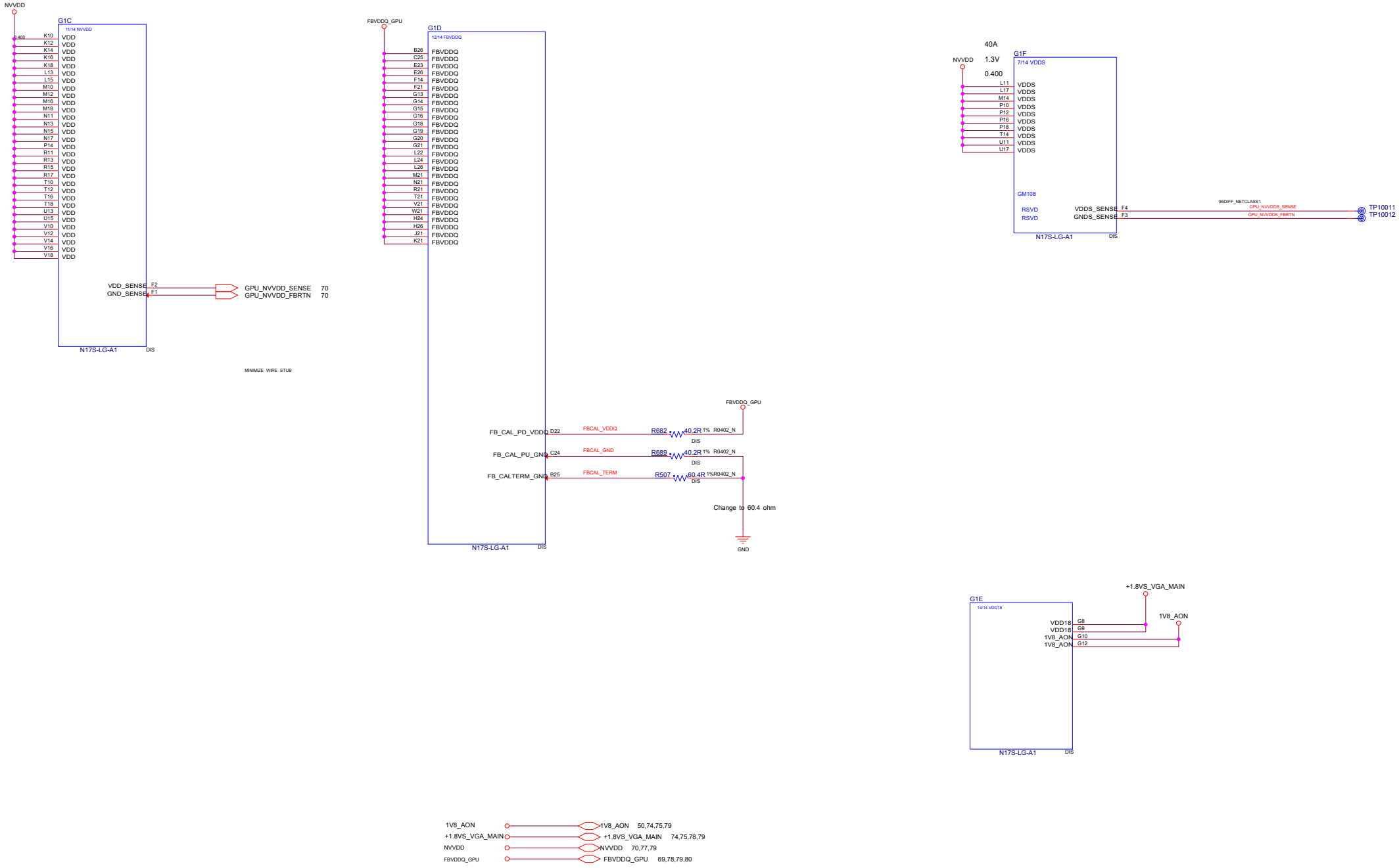
3nod三诺	Project: 520S-13	
	Engineer: *Jason*	
Size: B	Title: NA	Rev: V01
Date: Monday, April 10, 2017	Sheet 73 of 81	



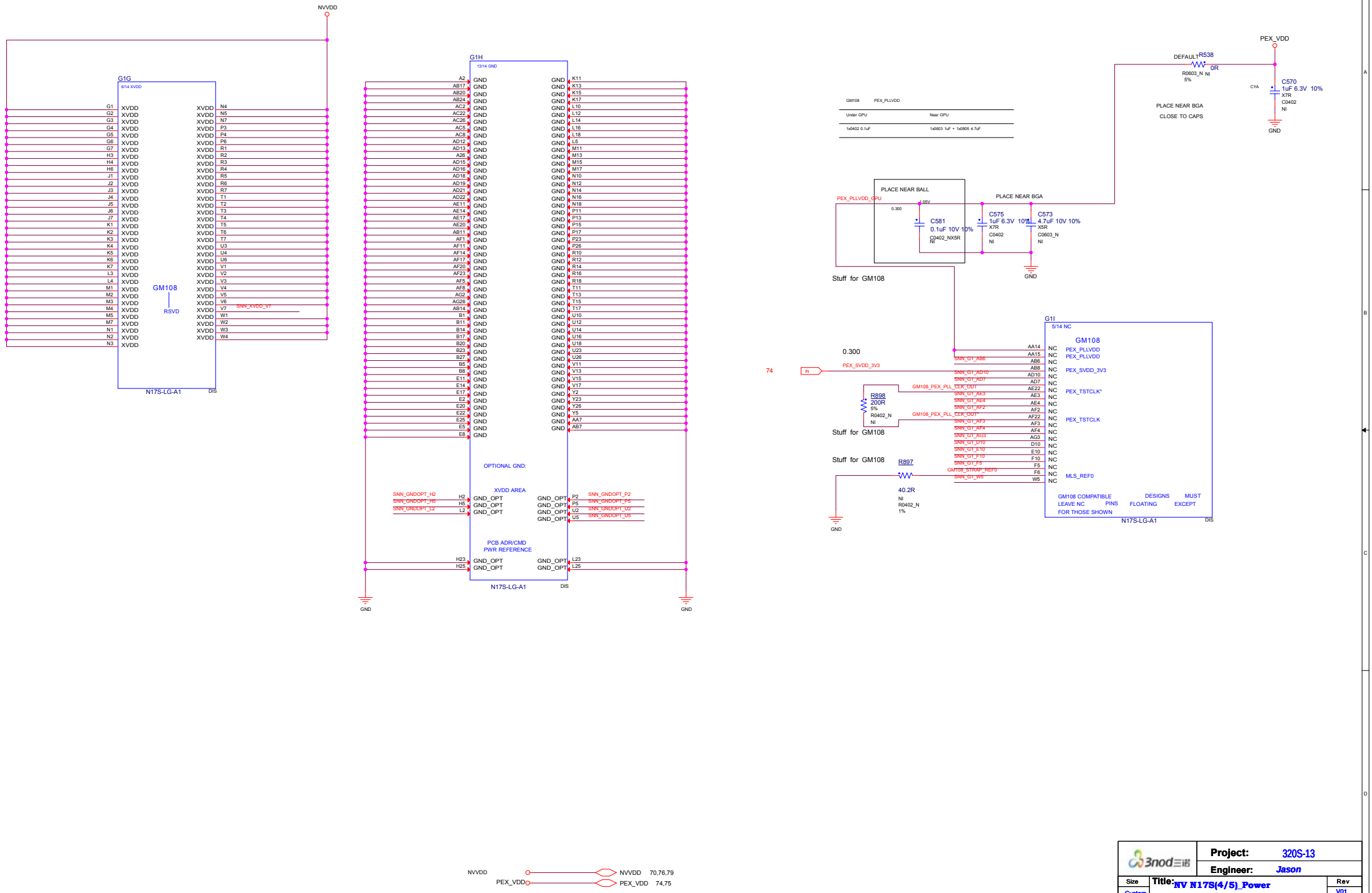
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NV N17S(1/5)_PCIE/DP	Rev: V01
Date: Monday, April 10, 2017	Sheet 74 of 81	



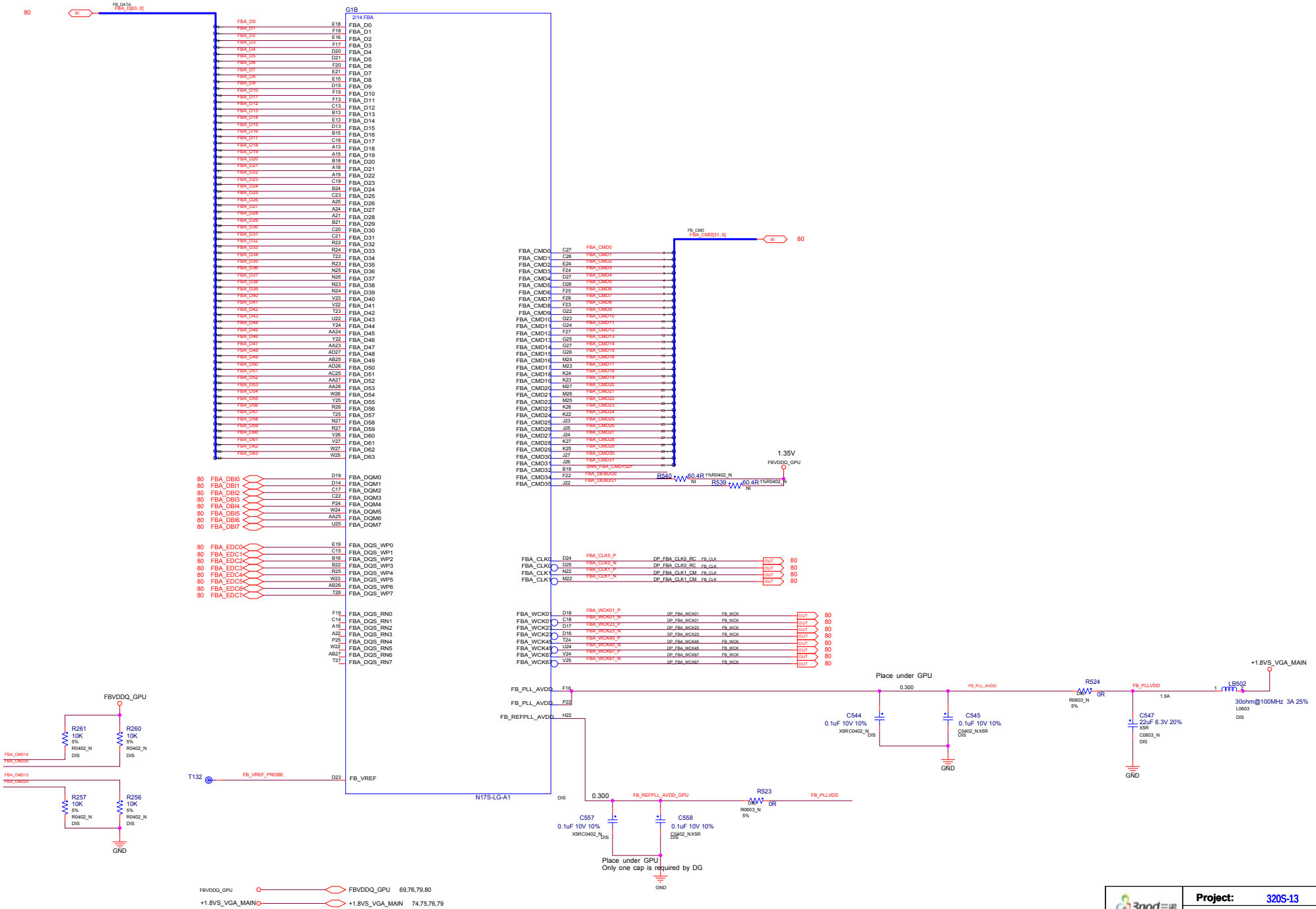
Density	Vendor	PN	Strap	Strap2	Strap1	Strap0
8Gb	Samsung	K4G80325FB-HC28	0X0	L	L	L
	Micron	MT51J256M32HF-70:A	0X1	L	L	H
	Hynix	H5GC8H24MJR-R0C	0X2	L	H	L
4Gb	Hynix	H5GC4H24AJR-R0C	0X6	H	H	L
	Samsung	K4G41325FE-HC28	0X7	H	H	H
	Micron	EDW4032BABG-70-F	0X8	L	L	M



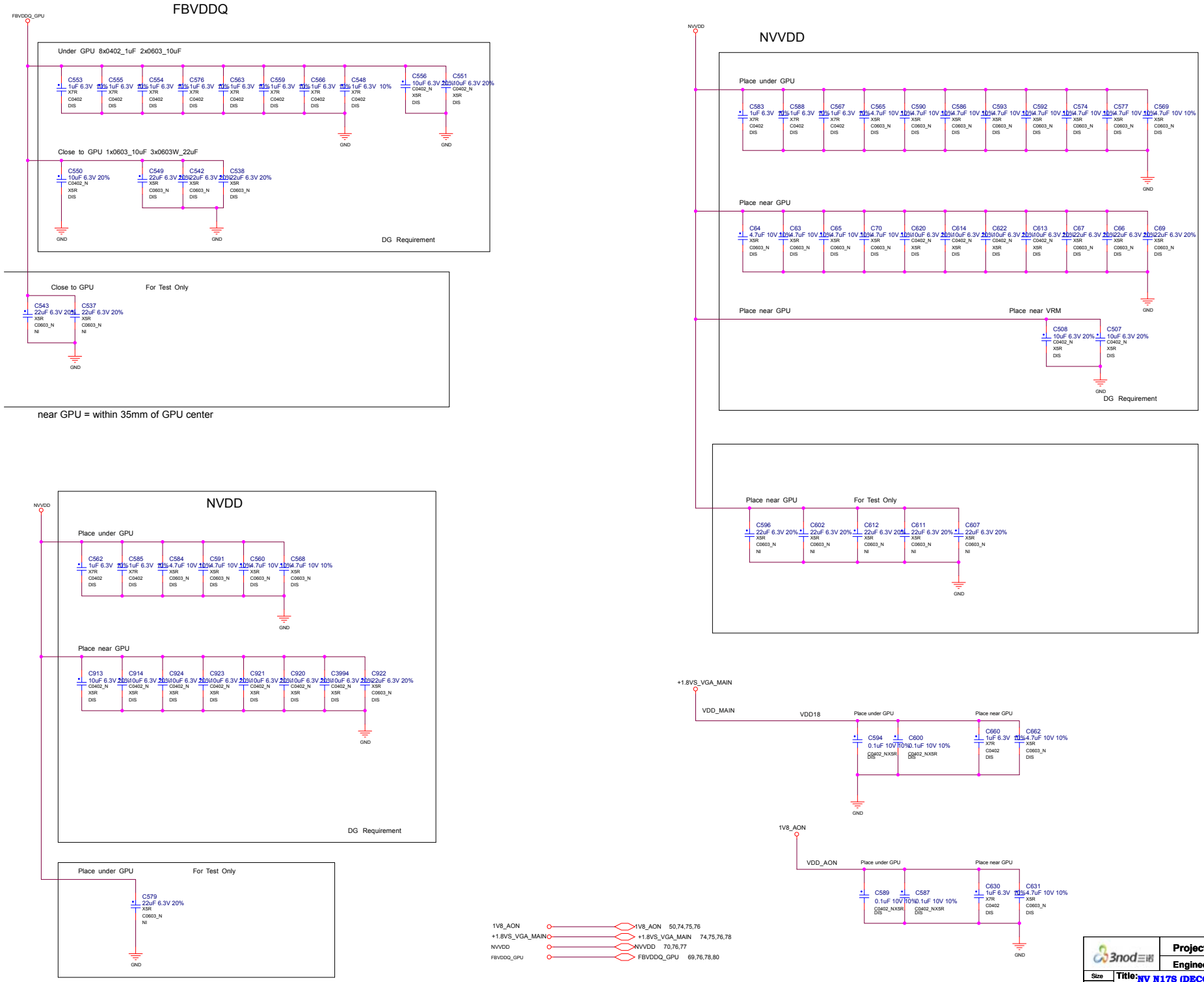
3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NV N17S(3/5)_Power/GND	Rev: V01
Date: Monday, April 10, 2017	Sheet 76 of 81	

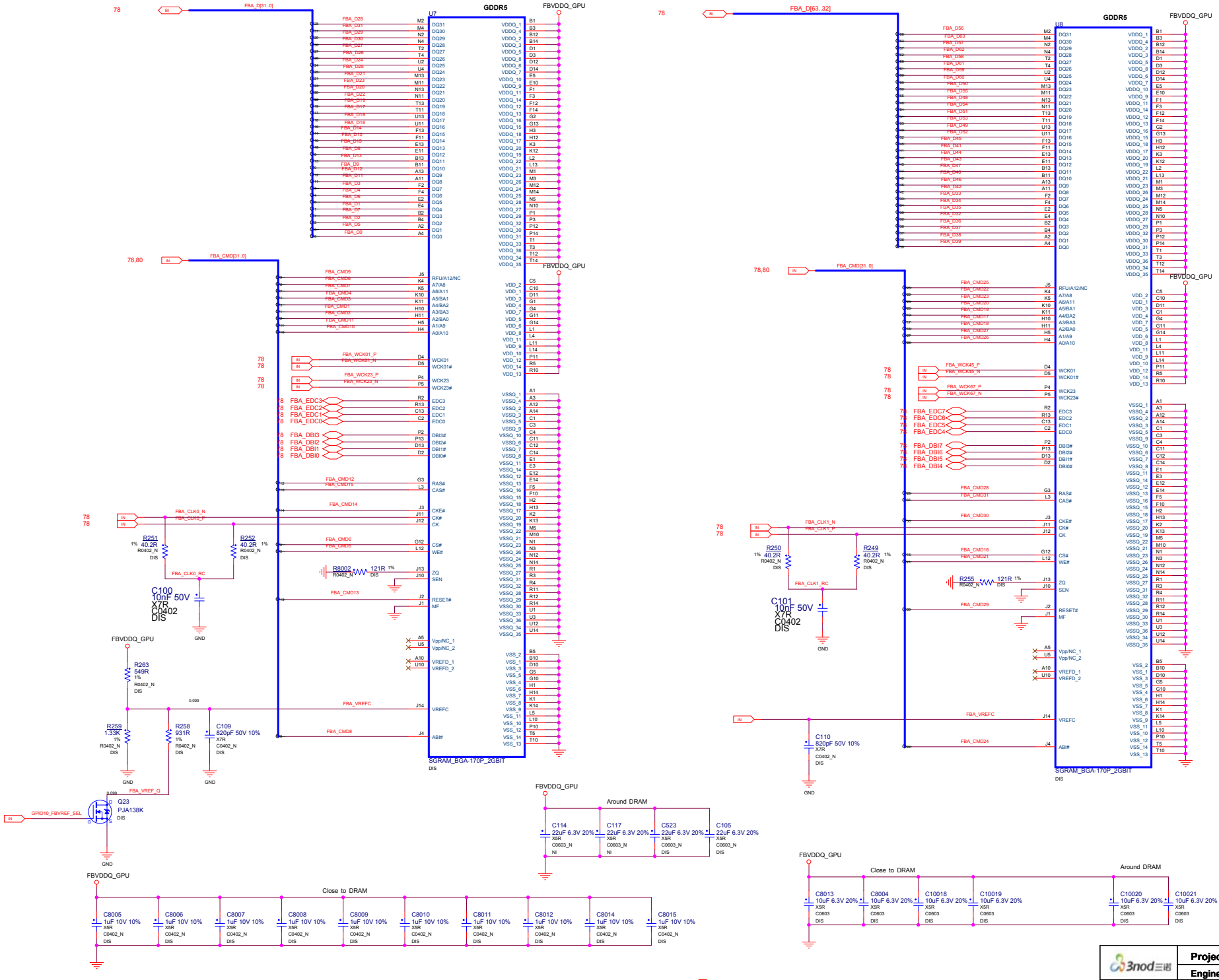


3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size: Custom	Title: NV N17S(4/5)_Power	Rev: V01
Date: Monday, April 10, 2017	Sheet 77 of 81	



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size C	Title: NV N17S(5/5)_MEM	Rev V01
Date: Monday, April 10, 2017	Sheet 78 of 81	


FBVDDQ
FBVDDQ_GPU
Under GPU 8x0402_1uF 2x0603_10uF
C553 1uF 6.3V 10% X7R C0402 DIS
C555 1uF 6.3V 10% X7R C0402 DIS
C554 1uF 6.3V 10% X7R C0402 DIS
C576 1uF 6.3V 10% X7R C0402 DIS
C563 1uF 6.3V 10% X7R C0402 DIS
C559 1uF 6.3V 10% X7R C0402 DIS
C566 1uF 6.3V 10% X7R C0402 DIS
C548 1uF 6.3V 10% X7R C0402 DIS
C556 10uF 6.3V 20% C0402_N X5R DIS
C551 10uF 6.3V 20% C0402_N X5R DIS
GND
Close to GPU 1x0603_10uF 3x0603W_22uF
C550 10uF 6.3V 20% C0402_N X5R DIS
C549 22uF 6.3V 20% X5R C0603_N DIS
C542 22uF 6.3V 20% X5R C0603_N DIS
C538 22uF 6.3V 20% X5R C0603_N DIS
DG Requirement
Close to GPU
For Test Only
C543 22uF 6.3V 20% X5R C0603_N NI
C537 22uF 6.3V 20% X5R C0603_N NI
near GPU = within 35mm of GPU center
NVVDD
Place under GPU
C583 1uF 6.3V 10% X7R C0402 DIS
C588 1uF 6.3V 10% X7R C0402 DIS
C567 1uF 6.3V 10% X7R C0402 DIS
C565 4.7uF 10V 10% X5R C0603_N DIS
C590 4.7uF 10V 10% X5R C0603_N DIS
C586 4.7uF 10V 10% X5R C0603_N DIS
C593 4.7uF 10V 10% X5R C0603_N DIS
C592 4.7uF 10V 10% X5R C0603_N DIS
C574 4.7uF 10V 10% X5R C0603_N DIS
C577 4.7uF 10V 10% X5R C0603_N DIS
C569 4.7uF 10V 10% X5R C0603_N DIS
Place near GPU
C64 4.7uF 10V 10% X5R C0603_N DIS
C63 4.7uF 10V 10% X5R C0603_N DIS
C65 4.7uF 10V 10% X5R C0603_N DIS
C70 4.7uF 10V 10% X5R C0603_N DIS
C620 10uF 6.3V 20% C0402_N X5R DIS
C614 10uF 6.3V 20% C0402_N X5R DIS
C622 10uF 6.3V 20% C0402_N X5R DIS
C613 10uF 6.3V 20% C0402_N X5R DIS
C67 22uF 6.3V 20% X5R C0603_N DIS
C66 22uF 6.3V 20% X5R C0603_N DIS
C69 22uF 6.3V 20% X5R C0603_N DIS
Place near GPU
Place near VRM
C508 10uF 6.3V 20% C0402_N X5R DIS
C507 10uF 6.3V 20% C0402_N X5R DIS
DG Requirement
Place near GPU
For Test Only
C596 22uF 6.3V 20% X5R C0603_N NI
C602 22uF 6.3V 20% X5R C0603_N NI
C612 22uF 6.3V 20% X5R C0603_N NI
C611 22uF 6.3V 20% X5R C0603_N NI
C607 22uF 6.3V 20% X5R C0603_N NI
NVVDD
Place under GPU
C562 1uF 6.3V 10% X7R C0402 DIS
C585 1uF 6.3V 10% X7R C0402 DIS
C584 4.7uF 10V 10% X5R C0603_N DIS
C591 4.7uF 10V 10% X5R C0603_N DIS
C560 4.7uF 10V 10% X5R C0603_N DIS
C568 4.7uF 10V 10% X5R C0603_N DIS
Place near GPU
C913 10uF 6.3V 20% C0402_N X5R DIS
C914 10uF 6.3V 20% C0402_N X5R DIS
C924 10uF 6.3V 20% C0402_N X5R DIS
C923 10uF 6.3V 20% C0402_N X5R DIS
C921 10uF 6.3V 20% C0402_N X5R DIS
C920 10uF 6.3V 20% C0402_N X5R DIS
C3994 10uF 6.3V 20% C0402_N X5R DIS
C922 22uF 6.3V 20% X5R C0603_N DIS
DG Requirement
Place under GPU
For Test Only
C579 22uF 6.3V 20% X5R C0603_N NI
+1.8VS_VGA_MAIN
VDD_MAIN
VDD18
Place under GPU
Place near GPU
C594 0.1uF 10V 10% C0402_NX5R DIS
C600 0.1uF 10V 10% C0402_NX5R DIS
C660 1uF 6.3V 10% X7R C0402 DIS
C662 4.7uF 10V 10% X5R C0603_N DIS
1V8_AON
VDD_AON
Place under GPU
Place near GPU
C589 0.1uF 10V 10% C0402_NX5R DIS
C587 0.1uF 10V 10% C0402_NX5R DIS
C630 1uF 6.3V 10% X7R C0402 DIS
C631 4.7uF 10V 10% X5R C0603_N DIS
1V8_AON 1V8_AON 50,74,75,76
+1.8VS_VGA_MAIN +1.8VS_VGA_MAIN 74,75,76,78
NVVDD NVVDD 70,76,77
FBVDDQ_GPU FBVDDQ_GPU 69,76,78,80
Project: 320S-13
Engineer: Jason
Size C
Title: NV N17S (DECOUPLING)
Rev V01
Date: Monday, April 10, 2017
Sheet 79 of 81



3nod三诺	Project: 320S-13	
	Engineer: Jason	
Size C	Title: VRAM (GDDR5)	Rev V01
Date: Monday, April 10, 2017	Sheet 80 of 81	

3nod三泰	Project: 320S-13	
	Engineer: Jason	
Size D	Title: RSVD	Rev V01
Date: Monday, April 10, 2017	Sheet 81 of 81	